

# Introduction to the Special Issue on the 2008 IEEE International Solid-State Circuits Conference

**T**HE IEEE International Solid-State Circuits Conference (ISSCC) is the foremost global forum for presenting advances in solid-state circuits and systems-on-a-chip. Every year since its very first issue, the IEEE JOURNAL OF SOLID-STATE CIRCUITS has highlighted some well-received papers from the most recent ISSCC in special issues. This special issue is for the ISSCC conference held in San Francisco, CA, February 3–7, 2008. Session chairs and co-chairs initially recommended papers for publication, with final decision for inclusion based on peer review.

## I. HIGH-PERFORMANCE DIGITAL PAPERS

Five papers come from the high-performance digital sessions of ISSCC 2008. Microprocessors have always represented some of the industry's most important circuit and system design efforts, and 2008 was no different. This issue features descriptions of two new enterprise processors. Konstadinidas *et al.* describe a third generation SPARC processor employing speculation and supporting transactional memory semantics. It contains 16 cores and can execute 32 threads in a 65 nm technology. Stackhouse *et al.* show Tukwila, a quad-core Itanium processor in 65 nm that puts a record 2.05 billion transistors on a single chip.

Two papers focus their attention on overcoming dynamic variability and soft errors. Das *et al.* present RazorII, a 64b processor in a 130 nm technology that actively detects and corrects for process, voltage, and temperature variations. Bowman *et al.* present circuits in a 65 nm test chip that detect and recover from timing errors as well as simplify the management of signal metastability. Both sets of techniques allow dynamic voltage scaling to reduce the overhead of design margins and increase performance efficiency.

Finally, clocking of large processors has traditionally consumed significant area, power, and design effort. Chan *et al.* show a modified Cell Broadband Engine Processor incorporating a resonant global clock distribution that offers lower power and full functionality over a 20% range in clock frequencies.

## II. LOW-POWER DIGITAL PAPERS

Eight papers have been included in this section, selected from the low-power digital design sessions at ISSCC 2008. These papers detail some of the leading-edge developments in energy-efficient and ultra-low-voltage circuit technologies, and cover a broad spectrum of topics ranging from sub-2 W microprocessors in 45 nm CMOS to subthreshold circuits and baseband/vision signal processing systems-on-chip.

The first paper, by Gerosa *et al.*, presents a 47-million transistor low-power Intel Architecture microprocessor for mobile

internet devices fabricated in 45 nm CMOS with a maximum thermal design power consumption of 2 W at 1.86 GHz.

The following three papers cover baseband signal processing. Ito *et al.* detail a  $9.3 \times 9.3 \text{ mm}^2$  baseband system-on-a-chip to support WCDMA with HSDPA and GSM/GPRS/EDGE fabricated in triple- $V_t$  65 nm CMOS that contains 20 power supply domains. Nilsson *et al.* describe an 11  $\text{mm}^2$  70 mW fully programmable baseband processor for mobile WiMAX and DVB-T/H fabricated in 0.12  $\mu\text{m}$  CMOS. Benkeser *et al.* present a 10.8 Mb/s Turbo Decoder ASIC targeted for digital HSDPA receiver applications fabricated in 130 nm CMOS that occupies 1.2  $\text{mm}^2$  and consumes 32 mW.

The next two papers present advances in ultra-low-voltage circuit technologies: Kaul *et al.* describe a 320 mV 411 GOPS/Watt ultra-low-voltage video motion estimation accelerator fabricated in 65 nm CMOS that consumes 56  $\mu\text{W}$ . Kwong *et al.* present a subthreshold microcontroller with integrated SRAM and a switched capacitor DC-DC converter operating down to 300 mV and consuming only 1  $\mu\text{W}$  of standby power.

An intelligent visual sensor system-on-a-chip with 2790 frames/second CMOS image sensor and 205 GOPS/Watt vision processor fabricated in 0.18  $\mu\text{m}$  CMOS is detailed in the following paper by Cheng *et al.* The final paper, by Kim *et al.*, describes a 36  $\text{mm}^2$  125 GOPS network-on-chip parallel processor targeted for real-time object recognition comprising an ARM10-compatible 32-bit processor with 8 SIMD clusters that consumes 583 mW in 0.13  $\mu\text{m}$  CMOS.

## III. MEMORY PAPERS

This section includes eight papers selected from the memory sessions at ISSCC 2008, which captured ever-accelerating scaling-down, enhanced performance, and lower power.

The first three papers discuss 45 nm SRAMs. SRAM scaling is a challenging area requiring design innovation due to critical issues such as transistor mismatch, threshold-voltage variation, PVT variation, and leakage reduction, all under low-voltage operation. The first paper, by Hamzaoglu *et al.*, addresses 45 nm SRAM scaling challenges in a high performance high- $\kappa$  metal-gate technology, achieving 3.5 GHz at 1.1 V on the Core 2 microprocessor. A forward-body-bias technique to enable low-voltage operation and also to deal with PVT variations is implemented in a 153 Mb SRAM core. The next paper, by Ramadurai *et al.*, presents another 45 nm SRAM in a 45 nm SOI SRAM technology with solutions for power reduction as well as leakage suppression for ASIC applications with a 450 ps access time. The third 45 nm SRAM paper, by Verma *et al.*, shows an innovative high-speed charge-transfer sense-amplifier circuit that improves access time by 34% with a very high-density bit-cell for low-power applications.

The next paper, by Somasekhar *et al.*, discusses an embedded dynamic memory aimed at replacing SRAM for on-die pro-

cessor caches. The area advantage of the eDRAM cell with enhanced cell performance makes 2T-DRAM competitive with eSRAM. The move from SOI to bulk successfully holds random access cycles, while increasing clock frequency to 2 GHz.

Three papers describe state-of-the-art NAND flash memory technologies and circuits. NAND is now the dominant technology for semiconductor storage and is challenging hard disk drives. These papers discuss recent flash memory advancements in array structure, multi-bit storage, and expanded endurance capability.

Cernea *et al.* provide a much enhanced program rate in a low-cost multi-level cell (MLC) by programming all bitlines simultaneously. The paper describes a 16 Gb MLC with 34 MB/s in MLC and 60 MB/s in SLC. Li *et al.* achieve a NAND flash design capable of storing eight levels in each memory cell, realizing three digital bits of storage per memory cell in a 56 nm technology. A program throughput of 8 MB/s is realized, which is comparable with the performance of 2 bit/cell designs previously reported at ISSCC. The final NAND memory paper, by Park *et al.*, builds two memory arrays stacked on top of each other, connecting to one level of peripheral devices through metal lines and vias. The design takes advantage of a 3D array of 43 nm NAND flash and 2 bit/cell storage to achieve  $0.0021 \mu\text{m}^2/\text{bit}$ .

The last paper, by Gastaldi *et al.*, presents a phase-change memory promising to become a unified memory technology, combining the characteristics of flash with the fast read and write operation of RAM. This paper demonstrates the feasibility of storing 2 bits/cell in a phase-change memory device.

#### IV. TECHNOLOGY DIRECTION PAPERS

This issue includes eight papers from the Technology Direction sessions of ISSCC 2008.

The first three papers discuss useful interfaces between CMOS integrated circuits and mechanical phenomena. Ruffieux *et al.* demonstrate a use of high quality bulk acoustic wave resonators as integral components in building a wireless CMOS RF transceiver. Guilar *et al.*, aiming at energy harvesting, convert vibration energies of a disk-shaped piezoelectric device to electrical energy, assisted by an efficient CMOS full-wave

rectifier. Colinet *et al.* report on a way to measure small displacements of a NEMS object: a displacement of a NEMS beam induces a change in its capacitance, which is detected by a CMOS detector circuit integrated in the same chip.

Works in the next two papers are aimed at wireless applications. Park *et al.* write on a wireless receiver for a cognitive radio application, which detects unused frequency spectra via a digitally-assisted analog energy detection method. Pletcher *et al.* report on a low-power wake-up receiver designed to activate a sensor node in wireless sensor networks. What they call an "uncertain-IF" architecture is one of keys to the receiver's low-power operation.

The next two papers discuss CMOS imager chips, intended for implantation in the human eye to help the blind see. Graf *et al.* discuss two chips: one has already been implanted in the human eye and partially restored vision; the other improves upon the first chip and is planned to be implanted. Rothermel *et al.* report on a CMOS imager chip, of which one important aim is to increase lifetime of the imager chip in an implanted environment. It has specific test features.

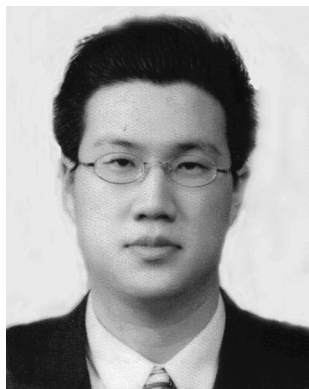
Finally, Schow *et al.* write on an implementation of a CMOS optical transceiver with 16 parallel transmitter channels and the equal number of parallel receiver channels, interfaced with an optical system consisting of 16-channel photodiodes and vertical cavity surface-emitting laser (VCSEL) arrays.

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He received the B.S. degree in physics from Seoul National University, Korea, in 1996, where he graduated *summa cum laude* with the Valedictorian Prize as well as the Presidential Prize, ranked top 1st across the Natural Science College, and also with the Physics Gold Medal (sole winner). Following 1.5 years of mandatory military service in the Republic of Korea Army, he proceeded to the California Institute of Technology, Pasadena, CA, where he received the M.S. degree in physics in 1999 working on general relativity and gravitational astrophysics, and the Ph.D. degree in electrical engineering in 2002, winning the Charles Wilts Doctoral Thesis Prize, Best Thesis Award in Electrical Engineering. His doctoral work examined the statistical physics of electrical circuits. He was the recipient of the IBM Doctoral Fellowship, IBM Faculty Partnership Award, IBM Research

Design Challenge Award, Li Ming Scholarship, Silver Medal in National Math Olympiad, and Fellow of the Korea Foundation

of Advanced Studies. He shared Harvard's Hoopes prize with William Franklin Andress. He was recognized by *MIT Technology Review* as among the world's top 35 young innovators in 2008 (TR35), for his group's work on CMOS RF biomolecular sensor using nuclear spin resonance to pursue early disease detection. The current focus of his research group at Harvard University is on: 1) RF, analog, and mixed-signal ICs; 2) GHz/THz one-dimensional plasmonic transport in quantum wires; 3) soliton and nonlinear wave electronics; 4) applications of CMOS ICs in biotechnology and medicine.

Dr. Ham's work experience includes the Caltech-MIT Laser Interferometer Gravitational Wave Observatory (LIGO), IBM T. J. Watson Research Center, IEEE conference technical program committees including the IEEE International Solid-State Circuits Conference (ISSCC) and the IEEE Asian Solid-State Circuits Conference (ASSCC), advisory board for the IEEE International Symposium on Circuits and Systems (ISCAS), international advisory board for the Institute for Nanodevices and Biosystems, and various industry, government, and academic technical advisory positions on subjects including ultrafast electronics, science and technology at the nanoscale, and the interface between biotechnology and microelectronics. He was a guest editor for the IEEE JOURNAL OF SOLID-STATE CIRCUITS in January 2009, and is a co-editor of *CMOS Biotechnology* (Springer, 2007).



**Hideto Hidaka** is Deputy General Manager, MCU Technology Division, MCU Business Group of Renesas Technology Corporation, Japan. He received the B.S., M.S., and Ph.D. degrees in electronic engineering from the University of Tokyo, Tokyo, Japan. He joined Mitsubishi Electric Corporation and in 2003 transferred to Renesas Technology Corporation, a merger by Mitsubishi Electric and Hitachi.

He has been engaged in the research and development of high-density DRAMs (256 Kb to 256 Mb), Cache-DRAM, SOI/DRAM, embedded-DRAM, high-speed embedded-Flash memory for MCU, Magnetic-RAM, and related embedded memory platforms for MCU/SOC. He was a visiting scientist at the Media Laboratory, Massachusetts Institute of Technology, Cambridge, MA, in 1987–1988. His current research interest includes embedded NV-memory technology for MCU/SOC, how and when embedded memory evolutions are implemented in real products, value/cost innovation patterns in semiconductor industry, and how to connect and collaborate in the “flat world” today.

Since 2000, Dr. Hidaka has served on the technical program committee for the ISSCC and is now the Memory Sub-Committee Chair. He has also been a member of the technical program committee for the Asian Solid-State Circuits Conference (A-SSCC) since 2005. He has authored or coauthored more than 50 journal papers and holds more than 400 patents, including 270 US patents and 107 Japanese patents, in semiconductor memory design and related technical fields.



**Ron Ho** (S'92–M'93–SM'08) is a Distinguished Principal Engineer at Sun Microsystems, working in the Sun Labs VLSI Research Group. He received the Ph.D. degree from Stanford University, Stanford, CA, in 2002, where he studied under Prof. Mark Horowitz and examined the scaling effects of long wires.

From 1993 to 2003, he was with Intel Corporation, Santa Clara, CA, where he worked on CPUs such as the Pentium II processor and the third-generation Itanium processor. There he focused on areas including data path automation, memory design, CAD for on-chip inductance, clocking, and process monitoring. In 2003, he joined Sun Labs in Menlo Park, CA, where he has been working on chip-to-chip and on-chip communication technologies, memory design, and asynchronous circuits. In 2004, Sun awarded him its Chairman's Award for Innovation.

Dr. Ho is a member of the technical program committees for the IEEE ISSCC, the IEEE Hot Interconnects Conference, the IEEE Symposium on Asynchronous Circuits and Systems, and the IEEE VLSI-DAT Conference. He was the General Chair of the 2008 IEEE/LEOS Workshop on Interconnections Within High-Speed Digital Systems, and has served as a guest associate editor for the JOURNAL OF QUANTUM ELECTRONICS. He has authored or coauthored over 35 technical papers in peer reviewed conferences and journals, and has 19 issued U.S. patents. He is a consulting Assistant Professor at Stanford University, and is a member of Tau Beta Pi and Phi Beta Kappa.



**Ram K. Krishnamurthy** (S'92–M'98–SM'03) received the B.E. degree in electrical engineering from Regional Engineering College, Trichy, India, in 1993, and the Ph.D. degree in electrical and computer engineering from Carnegie Mellon University, Pittsburgh, PA, in 1998.

Since 1998, he has been with Intel Corporation's Circuits Research Labs, Microprocessor Technology Labs, Hillsboro, OR, where he is currently a Senior Principal Engineer and heads the High-Performance and Low-Voltage Circuits research group. He holds 80 issued patents and has published two book chapters and over 75 conference/journal papers.

Dr. Krishnamurthy serves on the SRC ICSS Design Sciences Task Force and the program committees of the ISSCC, CICC, and SOCC conferences. He served as the Technical Program Chair/General Chair for the 2005/2006 IEEE International Systems-on-Chip Conference. He has received two Intel Achievement Awards, in 2004 and 2008, for the development of novel arithmetic circuit technologies and hardware encryption accelerators.