

**Engineering Sciences 154  
Laboratory Assignment 4**

## Enhancement Mode MOSFET Circuits

**Note: This is quite a long, but very important laboratory assignment. Take enough time -- at least two laboratory sessions -- to do each of the component tasks carefully.**

### **Abstract**

By configuring one or more of the devices on a 4007 chip, the basic electrical properties of enhancement mode MOSFET devices and circuits are observed and investigated. The following circuits are constructed and analyzed: NMOS common-source amplifier stages with active loads (*viz.*, a diode-connected NMOSFET and a PMOS current mirror); a CMOS inverter gate; and a CMOS transmission gate.

## The “Quadratic Model” of MOSFET Operation

In the text and lecture notes, a quadratic model of MOSFET operation is discussed extensively.<sup>1</sup> In particular, this model predicts the following drain current/drain-source voltage relationship in the *tetrode* region:

$$I_D = \mu C_{OX} \frac{W}{L} \left[ (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right] \quad [\text{Eq. 1}]$$

and the following drain current/drain-source voltage relationship in the *saturation* region:

$$I_{D,sat} = \mu C_{OX} \frac{W}{L} \frac{(V_{GS} - V_T)^2}{2} \quad [\text{Eq. 2}]$$

The product  $\mu C_{OX}$  is usual referred to as the *process* or *device conductivity* parameter K.

For the special case of a “diode-connected” MOSFET -- *viz.*, the case when the gate and drain are directly connected -- the characteristic becomes

$$I_{D,sat} = \mu C_{OX} \frac{W}{L} \frac{(V_{DS} - V_T)^2}{2} \quad [\text{Eq. 3}]$$

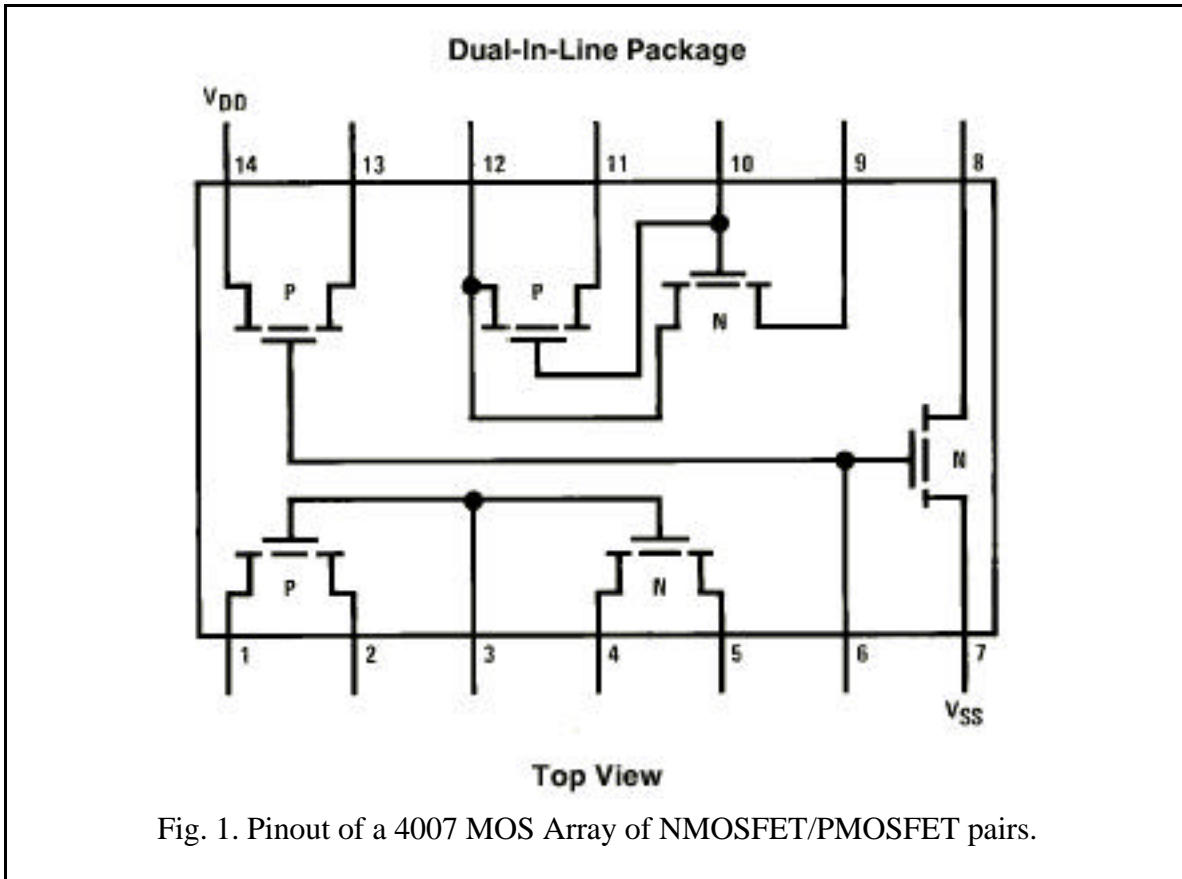
## Component Familiarization and Identification

The CD4007M/CD4007C consists of three complementary pairs of N- and P-channel enhancement mode MOS transistors suitable for series/shunt applications. All inputs are protected from static discharge by diode clamps to  $V_{DD}$  and  $V_{SS}$ . For proper operation the voltages at all pins must be constrained to be between  $V_{SS} - 0.3V$  and  $V_{DD} + 0.3V$  at all times. Note: All P-channel substrates are connected to  $V_{DD}$  and all N-channel substrates are connected to  $V_{SS}$ . Like all MOS devices, this chip is

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<sup>1</sup> See for example <http://schof.colorado.edu/~bart/book/models.htm>

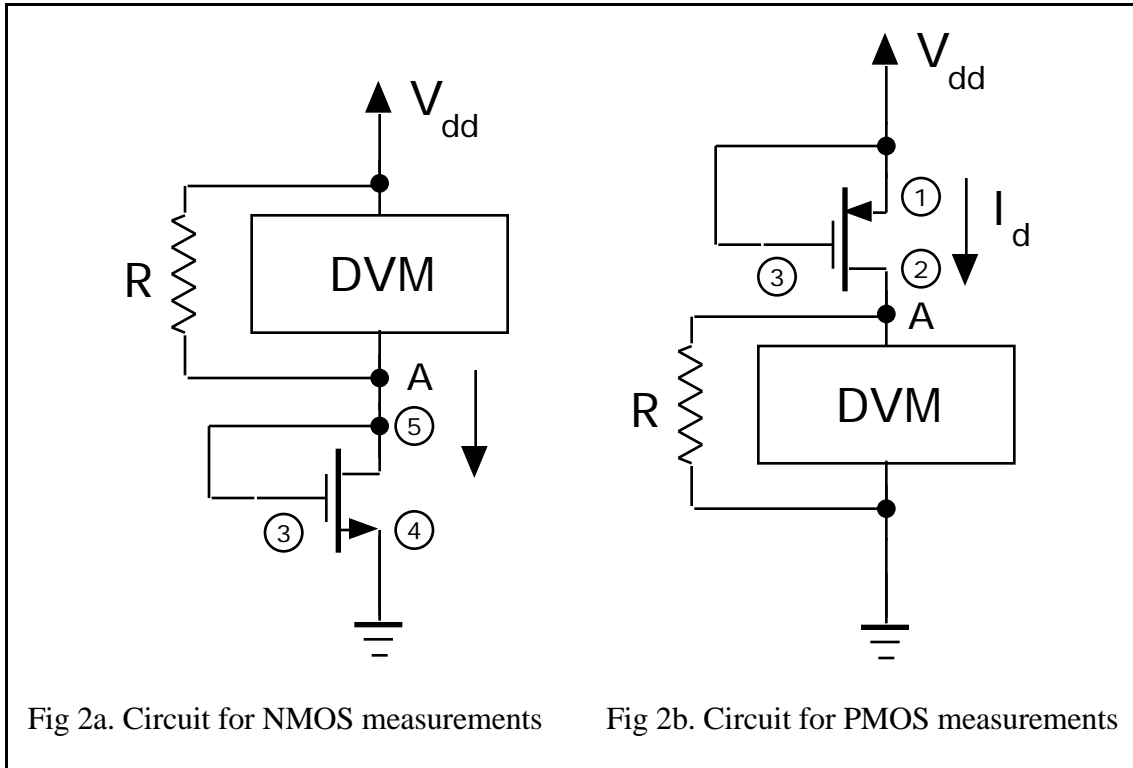
electrically fragile. Avoid handling it any more than necessary.



## Laboratory Tasks

### Task 1 – MOSFET Device Characteristics.

#### Subtask 1a – NMOS Device Voltage Threshold and Process Parameter



- Assemble the circuit as shown in Figure 2a above. Ensure that both substrate pins (*i.e.*, 7 and 14) are connected appropriately (*viz.*, pin 14 to  $V_{DD}$  and pin 7 to  $V_{SS} = \text{Gnd}$ ). All other pins may be left floating.
- Ensure that the supply voltage is precisely set to some convenient (and safe) value (say 10.0V), by connecting pins 4 and 5 momentarily and reading the DVM.
- Since the device in Figure 2a is “diode-connected,” Equation 3 should govern the behavior of the circuit. Thus, an appropriate set of measurements of drain current vs. drain to ground voltage may be used to find the device's threshold voltage,  $V_T$ , and process parameter,  $K$ . To this end measure  $V_{DS}$  (the DVM value minus the value measured in b) above) for several carefully selected resistors  $R$  and calculate in each case  $I_D$  from Ohms law

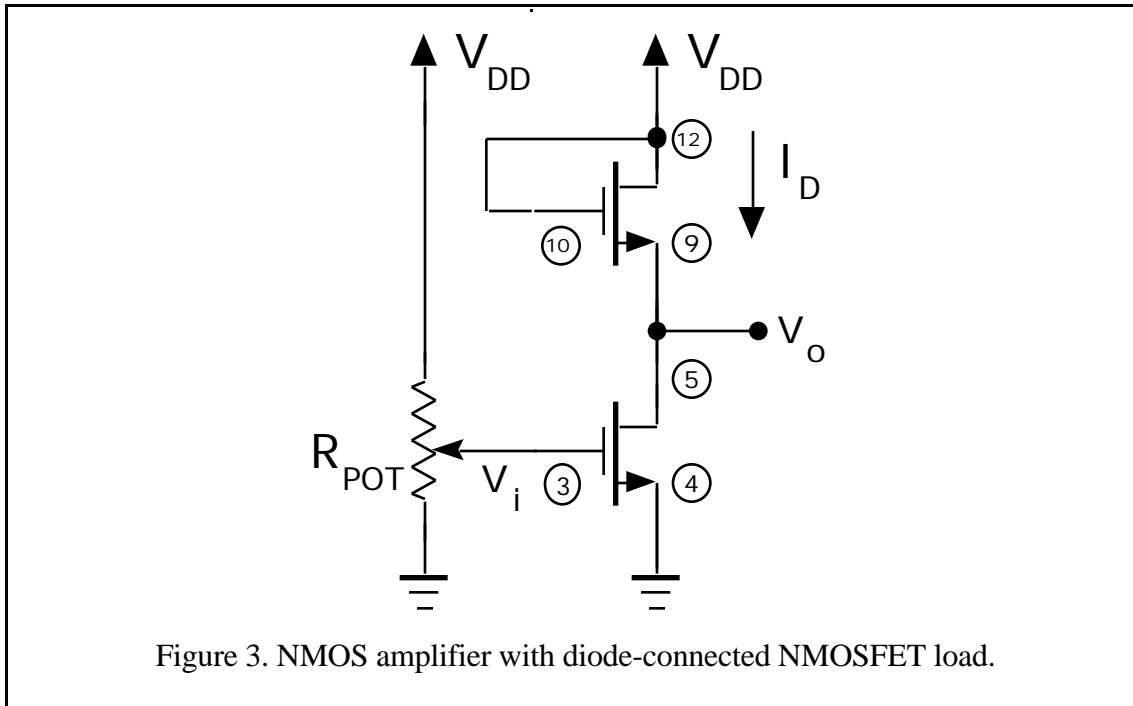
(you may need to consult the instruction book of DVM to find its internal resistance). Note: a very good way to rapidly check whether an enhancement transistor is good or bad is to measure how much drain current flows through the DVM (*i.e.*, the value of  $I_D$ , when  $R = \quad$ ).

- d) By plotting the data measured in c), find and report values of  $V_T$  and  $K$  (W/L).
- e) Are these  $V_T$  and  $K$  (W/L) values consistent with measurements on the other two NMOS transistors on the chip?

### **Subtask 1b – PMOSFET Voltage Threshold and Process Parameter**

- a) Assemble the circuit as shown in Figure 2b above. Ensure that both substrate pins (*i.e.*, 7 and 14) are connected appropriately (*viz.*, pin 14 to  $V_{DD}$  and pin 7 to  $V_{SS} = Gnu$ ). All other pins may be left floating.
- b) Ensure that the supply voltage is precisely set to some convenient (and safe) value (say 10.0V), by connecting pins 1 and 2 momentarily and reading the DVM.
- c) Since device in Figure 2b is also “diode-connected,” Equation 3 should govern the behavior of this circuit as well. Thus, an appropriate set of measurements of drain current vs. drain to ground voltage may be used to find the device's threshold voltage,  $V_T$ , and process parameter,  $K$ . To this end measure  $V_{DS}$  for several carefully selected resistors  $R$  and calculate in each case  $I_D$  from Ohms law.
- d) By plotting the data measured in c), find values of  $V_T$  and  $K$  (W/L).
- e) Are these  $V_T$  and  $K$  (W/L) values consistent with measurements on the other two PMOS transistors on the chip?

## Task 2 – NMOS Amplifier Stage with an Enhancement Load



- Assemble the circuit as shown in Figure 3 above. Ensure that both substrate pins (*i.e.*, 7 and 14) are connected appropriately (*viz.*, pin 14 to  $V_{DD}$  and pin 7 to  $V_{SS} = \text{Gnd}$ ). All other pins may be left floating. Use some convenient potentiometer value – say,  $R_{\text{POT}} = 100\text{k}$  .
- Using the DVM, measure, graph and report the complete  $v_i$  vs.  $v_o$  characteristic of this amplifier.
- Find and report the small signal voltage gain for the operating point at which maximum voltage swing is possible. How does your measured value compare with theoretical expectation (see Equation 5.84 in Sedra/Smith)?

### Task 3 – NMOS Amplifier Stage with a PMOS Current Mirror Load

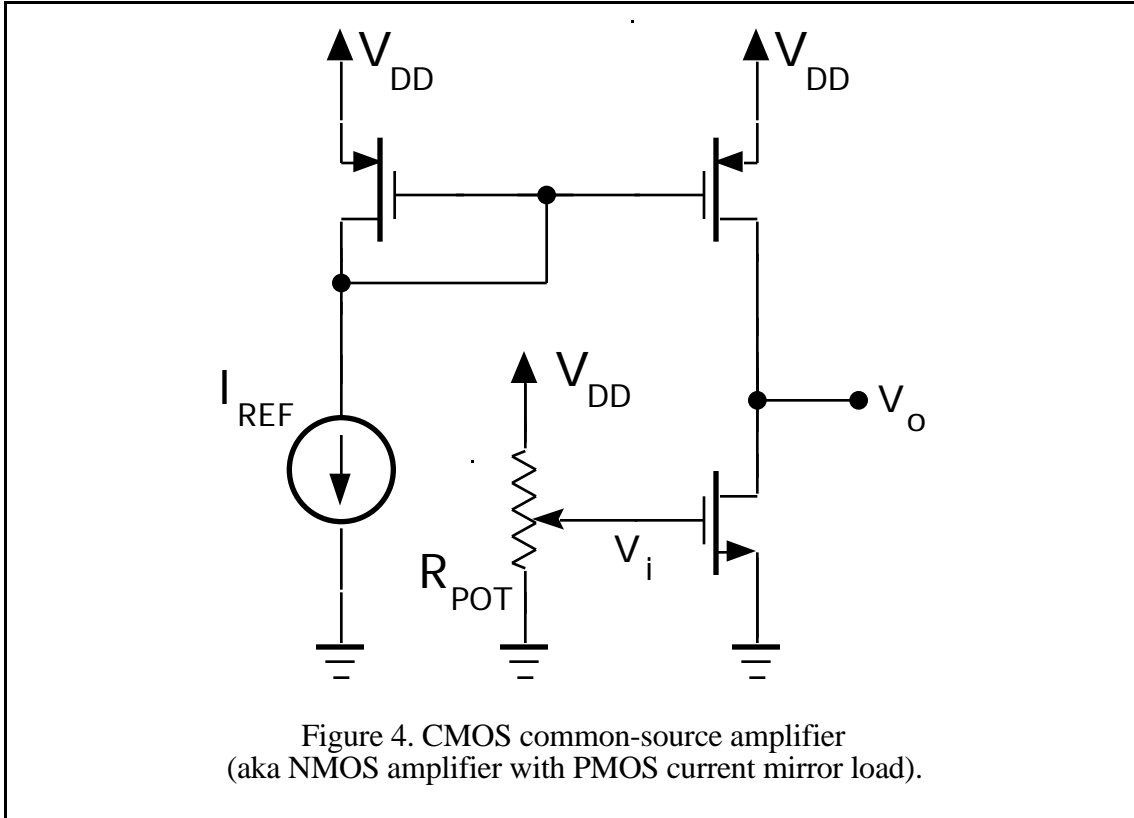


Figure 4. CMOS common-source amplifier (aka NMOS amplifier with PMOS current mirror load).

- Assemble the circuit as shown in Figure 4 above. Ensure that both substrate pins (*i.e.*, 7 and 14) are connected appropriately (*viz.*, pin 14 to  $V_{DD}$  and pin 7 to  $V_{SS} = \text{Gnd}$ ). All other pins may be left floating. Use some convenient potentiometer value – say,  $R_{POT} = 100\text{k}$  .
- Design a subcircuit to provide the current source  $I_{REF}$ . Choose  $I_{REF}$  so that the gainful transistor operates in the saturation region and  $v_o$  has a reasonable voltage swing.
- Using the DVM, measure, graph and report the complete  $v_i$  vs.  $v_o$  characteristic of this amplifier.
- Find and report the small signal voltage gain for the operating point at which maximum voltage swing is possible. How does your measured value compare with theoretical expectation (see Equation 5.61 in Sedra/Smith)?

- e) Compare your results for the two forms of active loading (*viz.*, Tasks 2 and 3)

#### Task 4 – CMOS Inverter Gate

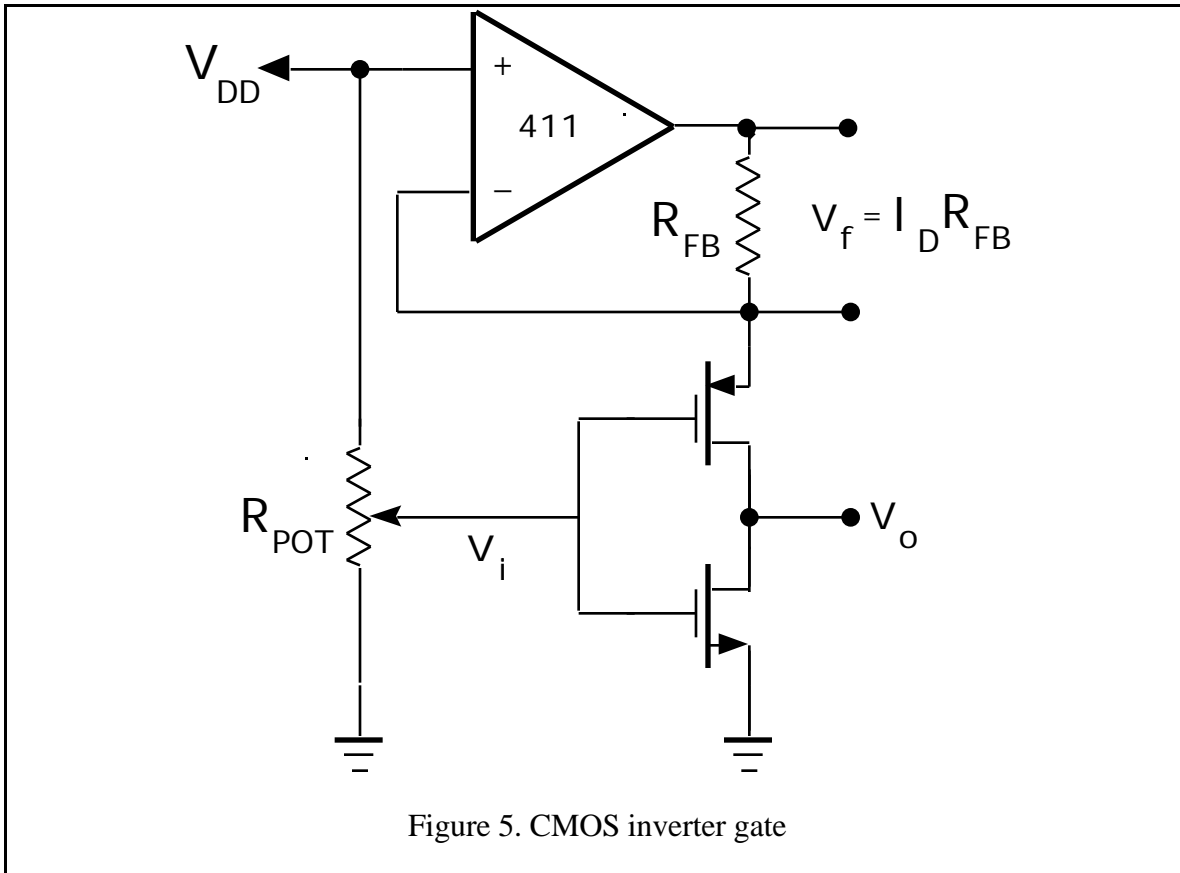


Figure 5. CMOS inverter gate

- a) Using one of the complementary pairs of enhancement mode MOS transistors on the 4007 chip, assemble the circuit as shown in Figure 5 above. Ensure that both substrate pins (*i.e.*, 7 and 14) are connected appropriately (*viz.*, pin 14 to  $V_{DD}$  and pin 7 to  $V_{SS} = \text{Gnd}$ ). All other pins may be left floating. Use some convenient potentiometer value – say,  $R_{POT} = 10\text{k}$  – and the feedback resistor  $R_{FB} = 1\text{k}$ .
- b) Vary potentiometer  $R_{POT}$  to change  $v_i$  from 0 V to  $V_{DD}$ . As you do this both  $I_D$  and  $v_o$  will change. The op-amp provides a means to determine  $I_D$  from Ohms law by measuring the floating voltage  $v_f$  across  $R_{FB}$ . After setting  $V$  somewhere

between 10 and 15 Volts, accurately measure it and make sure it does not change while you are gathering data.

- c) Measure and graph a set of data to obtain the complete transfer characteristic – viz.,  $v_O$  vs.  $v_i$  along with  $I_D$  vs.  $v_i$ . In particular, be sure to locate the switching thresholds where the slope of  $v_O$  vs.  $v_i$  is -1.
- d) In your report, construct the two graphs of the data from c) with a common independent axis (or simply align them one over the other) for  $v_i$ , so the relation between  $I_D$  and  $v_O$  can be easily seen. . Label your graph showing all significant points and regions of interest. Determine the logic low and high noise margins. Discuss how the NMOS and PMOS threshold voltages measured in Task 1 are significant, and relate them to your graphed data set.

### **Extra Credit Task or Mini-Miniproject.**

Design, build, test, and characterize a CMOS transmission gate using MOS transistors on the 4007 chip expectation (see Section 5.9 in Sedra/Smith).