

ENGINEERING SCIENCES 154  
ELECTRONIC DEVICES AND CIRCUITS  
SAMPLE FINAL EXAMINATION  
FALL TERM 2001-2002

NAME Some Possible Solutions

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- Please answer all of the questions in the spaces provided. If you need additional space, use the backs of the sheets.
  - Partial credit is achievable, **so include all of your calculations and clearly indicate what you are trying to do.**
  - Note that you have **modicum of choice** in the first question.
  - The relative credit assigned to each question is indicated as a *prudent time allocation*. That is, there is a possible total credit of **180**.
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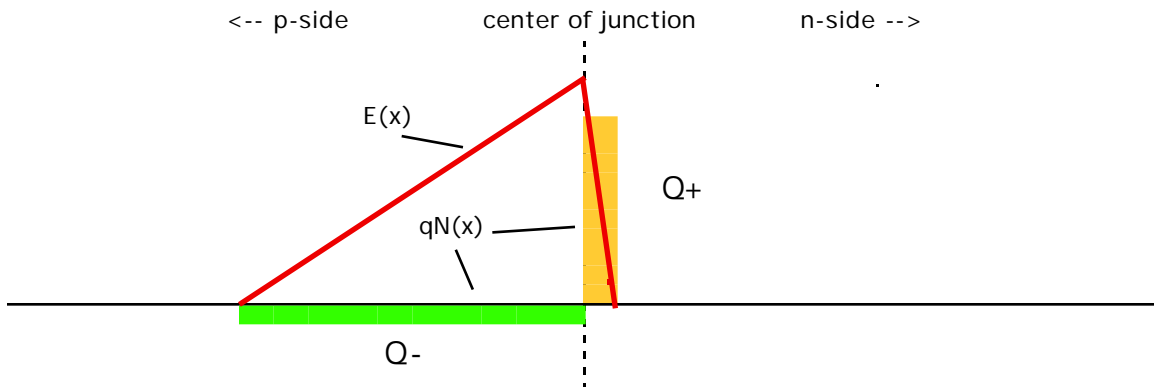
1. (Prudent time allocation = 90 minutes)

**Briefly** answer **NINE (9)** of the following **FOURTEEN (14)** questions:

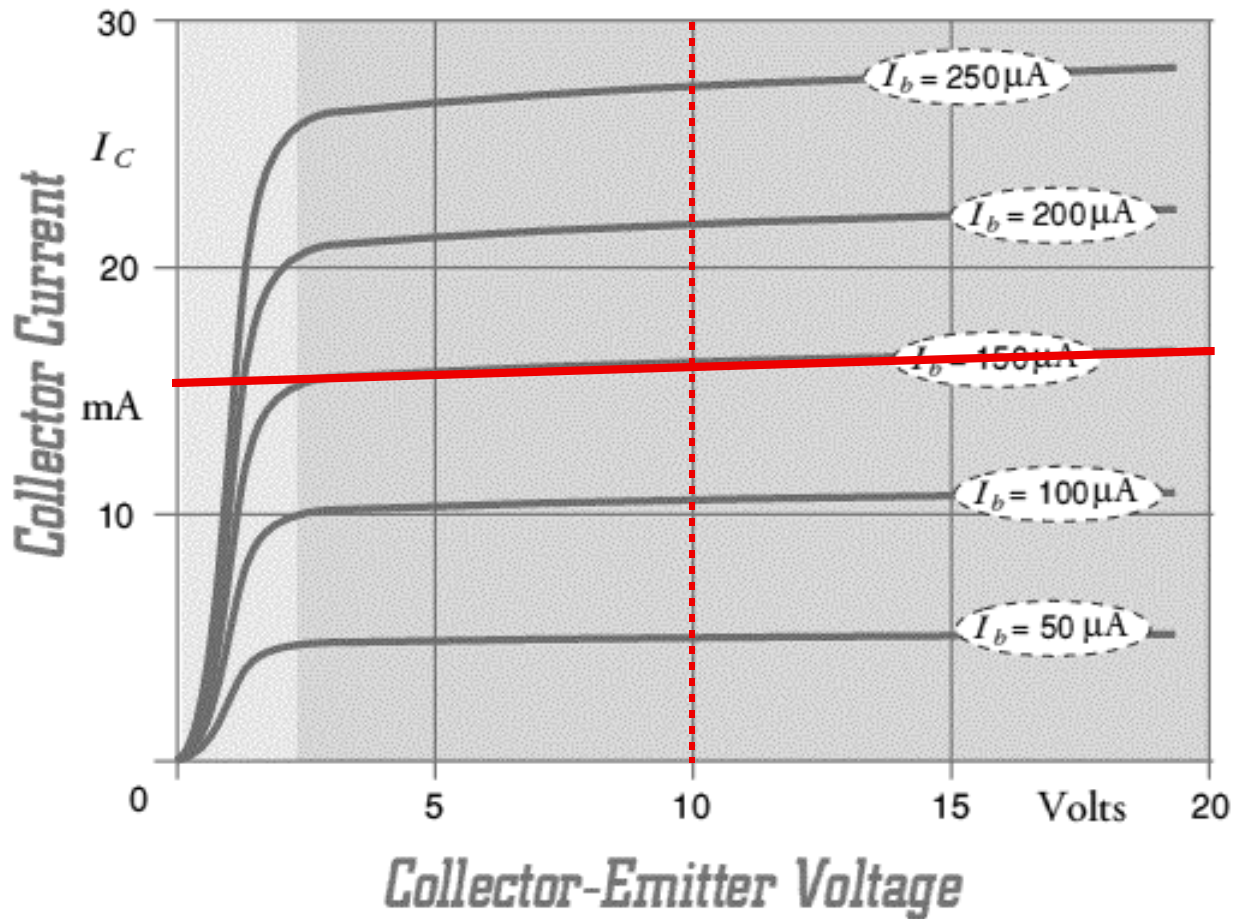
- In the space below, plot the **net charge density** (sign and magnitude) **and** the **built-in electric field** as a function of position along a line which intersects a pn homojunction at right angles. The n-side of the junction has a doping level that is 10 times that of the p-side (*i.e.*,  $N_D = 10 N_A$ ). Label and/or note important features.

**See discussion at:**

[www.deas.harvard.edu/courses/es154/lectures/lecture\\_2/pn\\_junction/pn\\_junction.html#space\\_charge](http://www.deas.harvard.edu/courses/es154/lectures/lecture_2/pn_junction/pn_junction.html#space_charge)



- b. Suppose that a particular BJT has the following collector current characteristic curve:



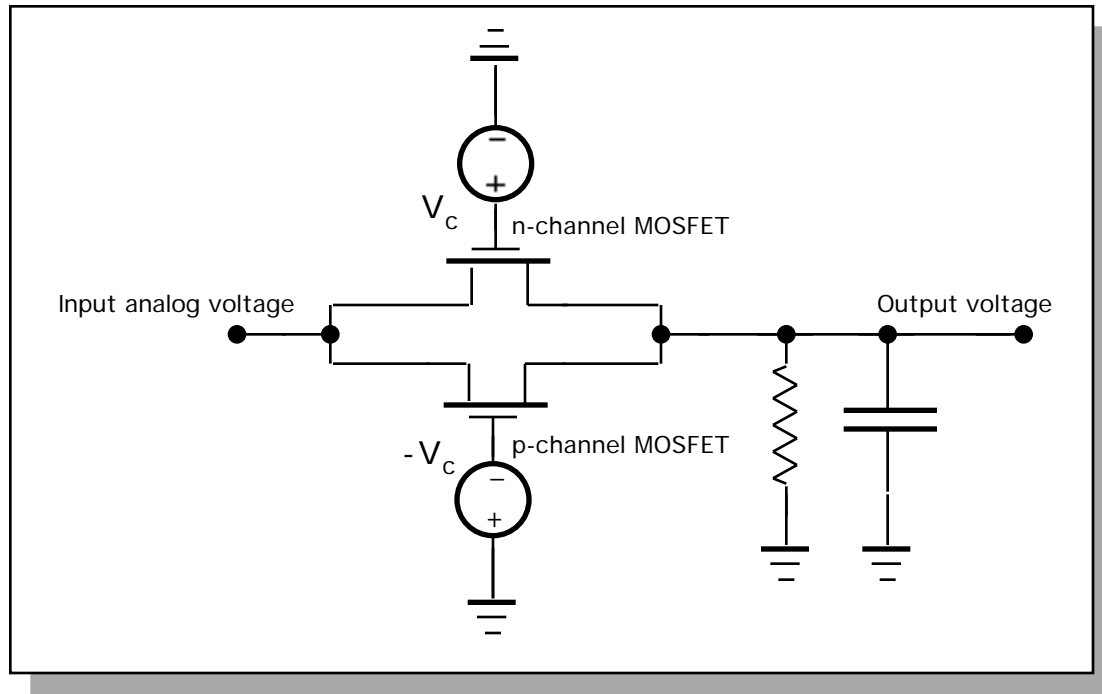
Using this characteristic, find the **common emitter current gain** (CECG) and the **common base current gain** (CBCG) of the transistor when it is operated in the “active mode.” Also find the Early voltage ( $V_A$ ) of the transistor.

$$= \frac{(16.0 - 10.05) \text{ mA}}{50 \mu\text{A}} = \frac{5.95}{50} \times 10^3 = 120$$

$$= \frac{120}{+1} = \frac{120}{121} = 0.992$$

$$V_A = \frac{I(0)}{[I(V_m) - I(0)]} V_m = \frac{15.5}{[16.5 - 15.5]} 20 \text{ V} = 310 \text{ V}$$

- c. What does the circuit illustrated below do? Explain how it does it..



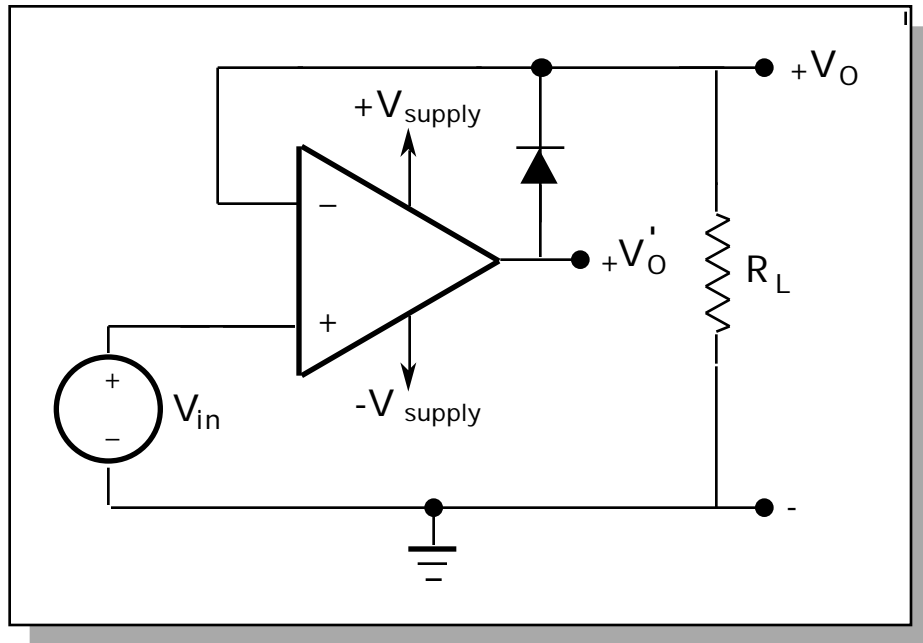
**See discussion at:**

[www.deas.harvard.edu/courses/es154/lectures/lecture\\_4/mosfet/mos\\_circuits/mos\\_circuits.html#trans\\_gate](http://www.deas.harvard.edu/courses/es154/lectures/lecture_4/mosfet/mos_circuits/mos_circuits.html#trans_gate)

- d. A **two-part** question about operational amplifier “offsets”
- i.) What is meant by the “input offset voltage” of an op amp? How is it measured?
  - ii.) What is meant by the “input offset current” of an op amp?

**See Section 2.9 Sedra & Smith and Laboratory Assignment 1.**

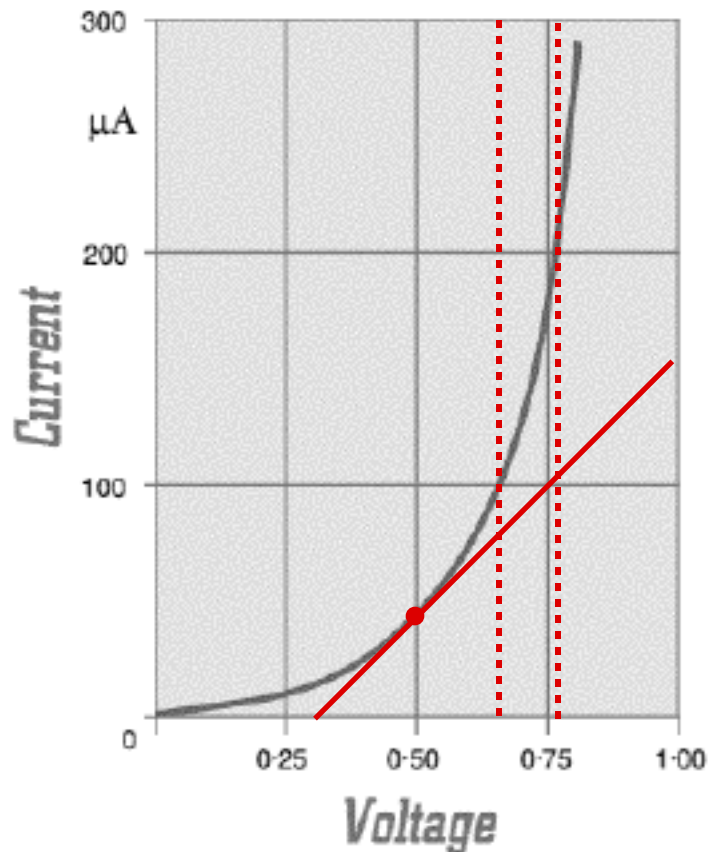
- e. The following circuit has been described as an “improved rectifier.” Explain.



**See discussion at:**

[www.deas.harvard.edu/courses/es154/lectures/lecture\\_2/diode\\_circuits/diode\\_app1.html#rectifier](http://www.deas.harvard.edu/courses/es154/lectures/lecture_2/diode_circuits/diode_app1.html#rectifier)

- f. For a diode with the characteristic depicted below, calculate the effective or small-signal resistance at a forward bias of 0.5 volts.



Slope Method:

$$r_{\text{eff}} = \frac{V}{I} = \frac{0.7 \text{ V}}{155 \mu\text{A}} = 4.5 \text{ k}$$

Analytic Method:

$$\text{Assume that } I(V_1) = I_0 \exp \frac{V}{V_T} - 1 \quad I_0 \exp \frac{V}{V_T}$$

$$\text{therefore } \frac{1}{r_{\text{eff}}} = \frac{d}{dV} I_0 \exp \frac{V}{V_T} = \frac{I(V)}{V_T} \quad \text{where } V_T = \frac{V_1 - V_2}{\ln \frac{I(V_1)}{I(V_2)}}$$

$$\text{From graph: } I(0.50 \text{ V}) = 45.5 \mu\text{A}; \quad I(0.66 \text{ V}) = 100 \mu\text{A}; \quad I(0.76 \text{ V}) = 200 \mu\text{A}$$

$$V_T = \frac{V_1 - V_2}{\ln \frac{I(V_1)}{I(V_2)}} = \frac{0.76 - 0.66}{\ln \frac{200}{100}} = \frac{0.10}{.693} = 0.144 \text{ V}$$

$$\frac{1}{r_{\text{eff}}} = \frac{I(V)}{V_T} = \frac{45.5 \mu\text{A}}{144 \text{ mV}} = \frac{1}{3.2 \text{ k}}$$

- g. In the space below, sketch a **complete** small signal equivalent circuit of a MOS transistor (assume that the **body** is not connected to the **source**). Identify each element of the equivalent circuit and give a “ball park” estimate of its magnitude.

**See discussion at:**

[www.deas.harvard.edu/courses/es154/lectures/lecture\\_4/mosfet/mos\\_models/mos\\_models.html#body\\_effect](http://www.deas.harvard.edu/courses/es154/lectures/lecture_4/mosfet/mos_models/mos_models.html#body_effect)

- h. In the space below, draw a **cascode amplifier** stage and briefly describe the advantages this configuration offers in circuit design.

**See discussion at:**

[www.deas.harvard.edu/courses/es154/lectures/lecture\\_5/lecture\\_5.html#cascode\\_amp](http://www.deas.harvard.edu/courses/es154/lectures/lecture_5/lecture_5.html#cascode_amp)

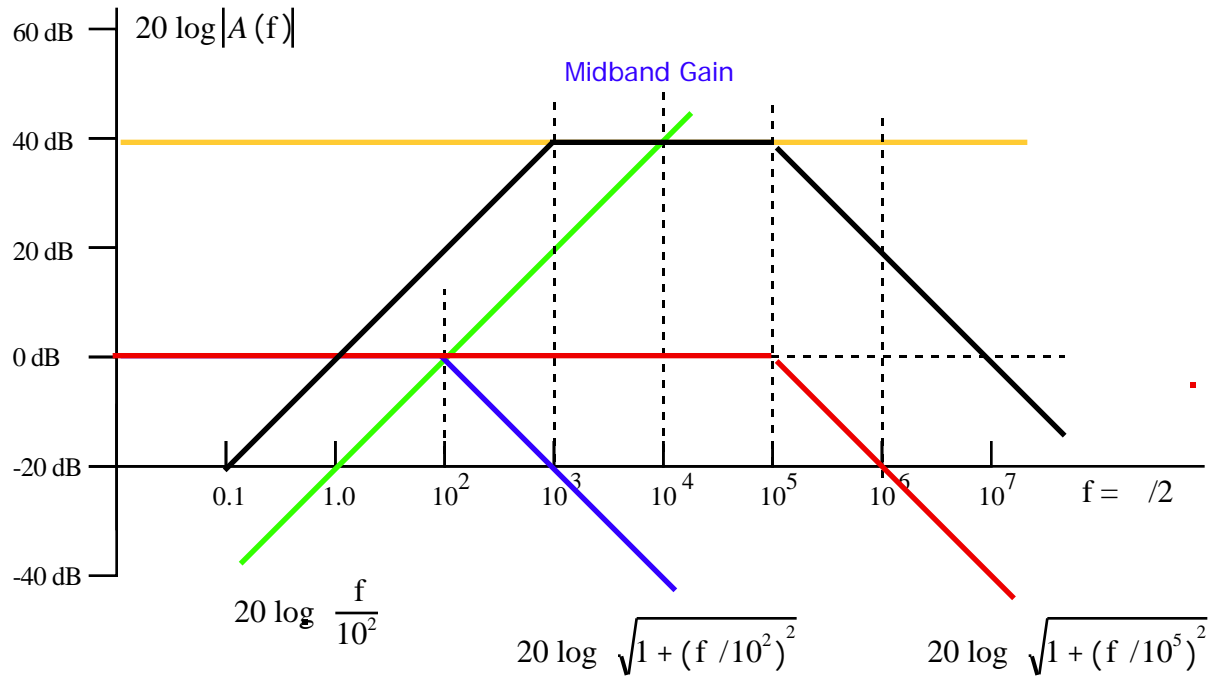
- i. An amplifier has the gain transfer function

$$A(s) = 10^2 \frac{s}{s + 2 \times 10^2} \frac{1}{1 + s/2 \times 10^5}$$

In the space below sketch a Bode plot for its **magnitude** and specify the midband gain, the lower 3-dB frequency and the upper 3-dB frequency.

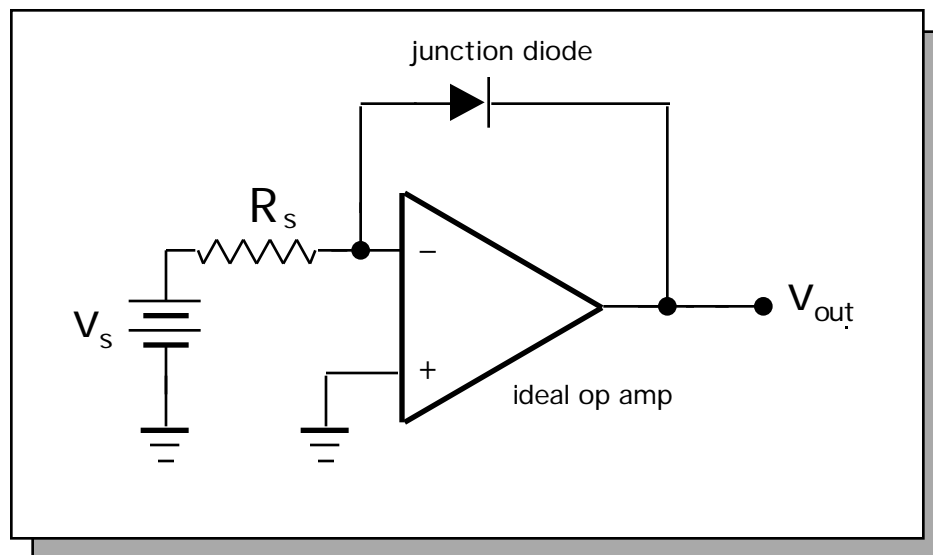
$$|A(f)| = 10^2 \frac{f/2 \times 10^2}{\sqrt{1 + (f/2 \times 10^2)^2}} \frac{1}{\sqrt{1 + (f/2 \times 10^5)^2}}$$

$$20 \log |A(f)| = 40 + 20 \log \frac{f}{10^2} - 20 \log \sqrt{1 + (f/10^2)^2} - 20 \log \sqrt{1 + (f/10^5)^2}$$



**See Section 7.1 and Example 7.1 in Sedra and Smith**

- j. The following circuit is used as a **temperature measuring device**. Find an expression for  $V_{out}$  as a function of the temperature to be measured.

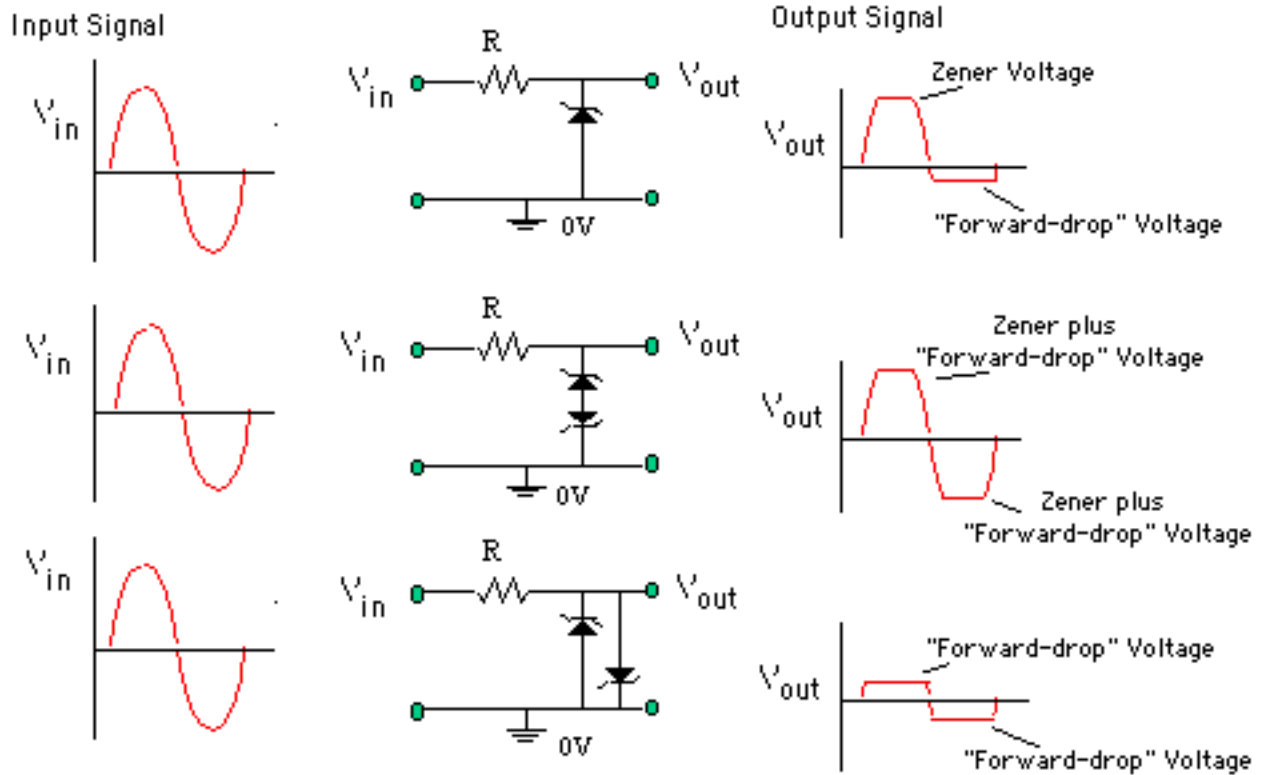


Assume that  $I(V) = I_0 \exp \frac{V}{n k T} - 1$

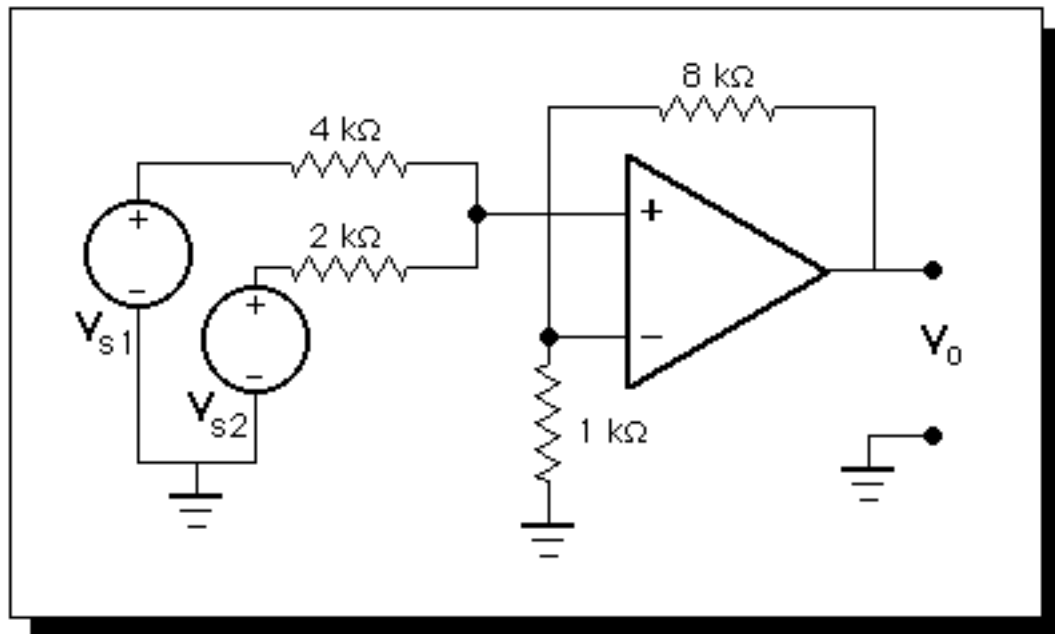
therefore  $\frac{V_S}{R_S} = I_0 \exp \frac{V_{OUT}}{n k T} - 1$

so that  $T = \frac{V_{OUT}}{n k \ln \frac{V_S}{I_0 R_S} + 1}$

k. Consider the three Zener diode circuits illustrated below. In the spaces provide, sketch a representation of the time dependent output signal for each of the three cases



1. In the following circuit, find  $V_o$  in terms of  $V_{s1}$  and  $V_{s2}$  using the ideal op amp model.



$$V_+ = V_{s2} + 2k \frac{V_{s1} - V_{s2}}{6k} = V_{s1} - 4k \frac{V_{s1} - V_{s2}}{6k} = \frac{V_{s1} + 2V_{s2}}{3}$$

$$V_- = \frac{1}{9} V_{OUT}$$

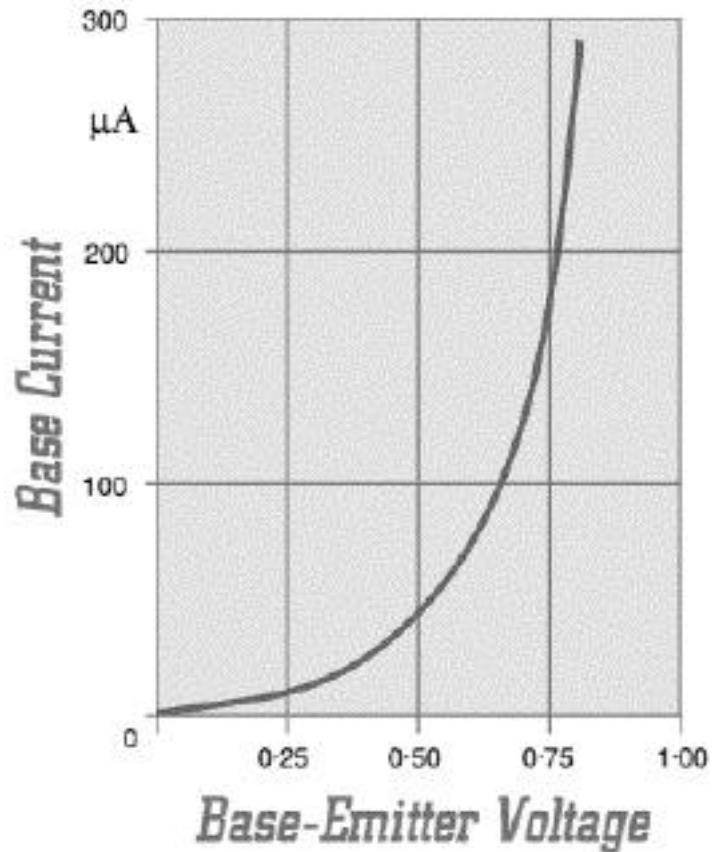
$$\text{therefore } V_{OUT} = 3(V_{s1} + 2V_{s2})$$

- m. Using expressions for the  $i_D$ - $v_{DS}$  characteristics of an enhancement mode, n-channel MOSFET (as derived in the text and lecture), derive expressions for the small-signal **transconductance**  $g_m$  in both the triode **and** saturation regions of operation.

**See discussion at:**

[www.deas.harvard.edu/courses/es154/lectures/lecture\\_4/mosfet/mos\\_models/mos\\_models.html](http://www.deas.harvard.edu/courses/es154/lectures/lecture_4/mosfet/mos_models/mos_models.html)

- n. The following important characteristic curves for a particular BJT which tells us a good deal about that device performance.



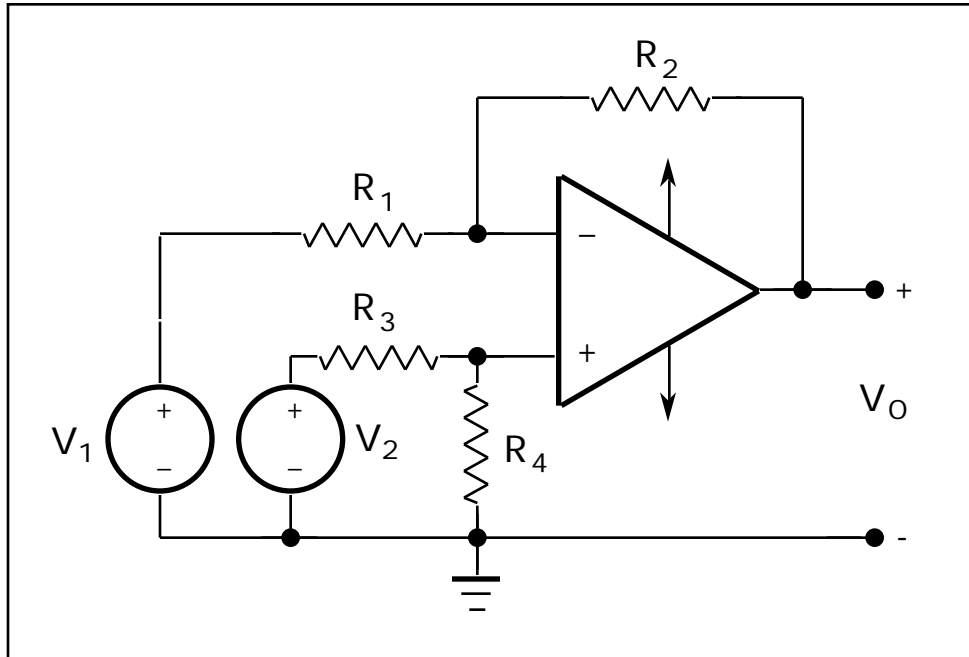
**Briefly** discuss the physics of this curve. What is the origin of this current? Why does it have the shape that it does? What does it tell us about the given transistor's performance?

**See discussion at:**

[www.deas.harvard.edu/courses/es154/lectures/lecture\\_3/collector\\_current/collector\\_current.html](http://www.deas.harvard.edu/courses/es154/lectures/lecture_3/collector_current/collector_current.html)

2. (Prudent time allocation = 15 minutes)

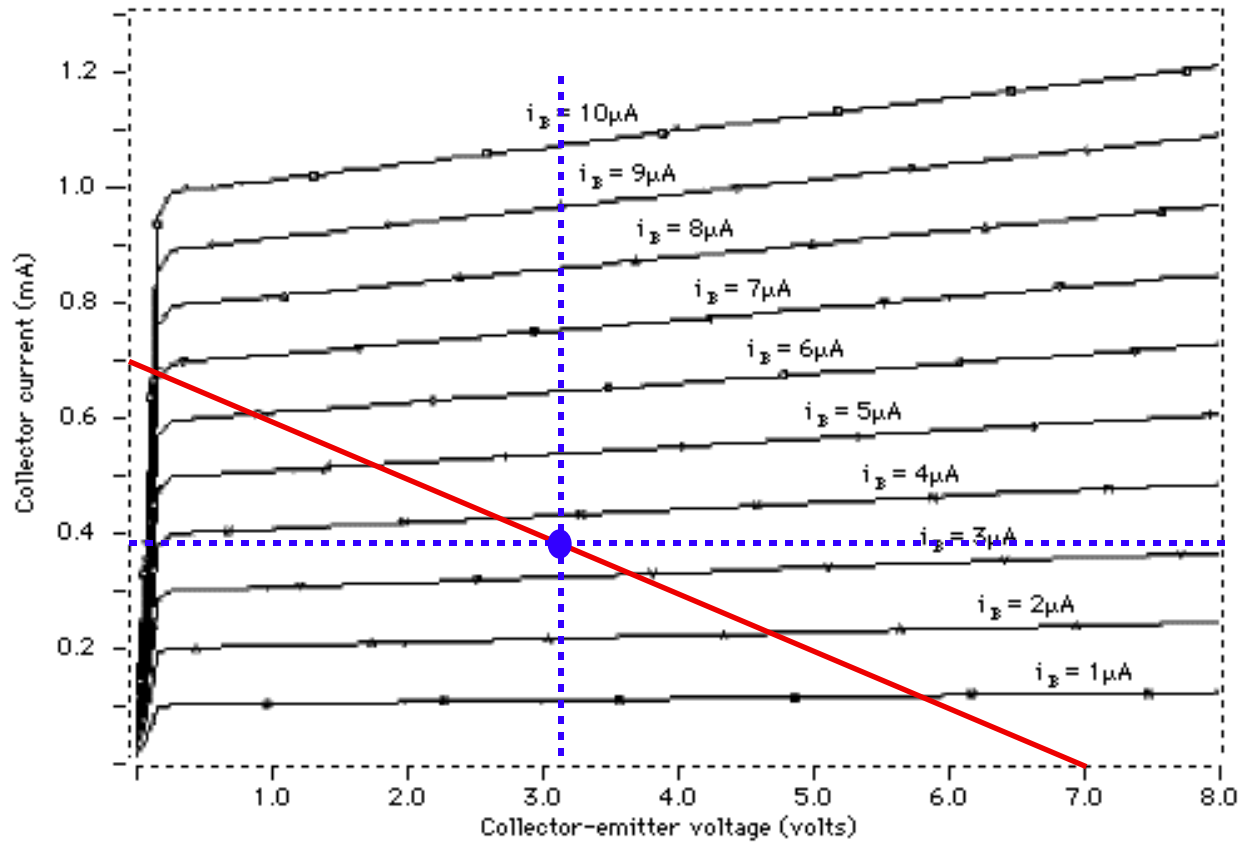
For the amplifier circuit shown below, find an expression for the output  $v_o$  in terms of the two inputs  $v_1$  and  $v_2$ . From this expression find expressions for the differential gain  $G_d$ , the common-mode gain  $G_{CM}$  and the common-mode rejection ratio CMRR.



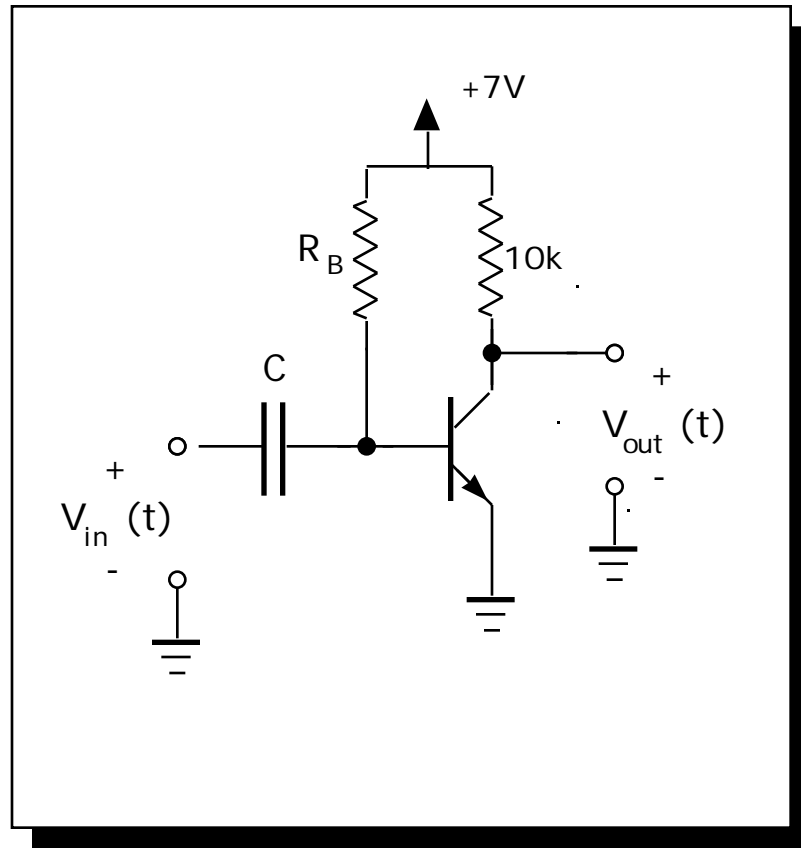
$$\begin{aligned} \frac{v_- - v_1}{R_1} &= \frac{v_o - v_-}{R_2} & v_- &= \frac{R_2}{R_1 + R_2} v_1 + \frac{R_1}{R_1 + R_2} v_o \\ v_+ &= \frac{R_4}{R_3 + R_4} v_2 \\ v_+ &= v_- & \frac{R_4}{R_3 + R_4} v_2 &= \frac{R_2}{R_1 + R_2} v_1 + \frac{R_1}{R_1 + R_2} v_o \\ v_o &= \frac{R_1 + R_2}{R_1} \frac{R_4}{R_3 + R_4} v_2 - \frac{R_2}{R_1 + R_2} v_1 \\ &= \frac{R_1 + R_2}{R_1} \frac{R_4}{R_3 + R_4} v_{cm} + \frac{v_d}{2} - \frac{R_2}{R_1 + R_2} v_{cm} - \frac{v_d}{2} \\ &= \frac{v_d}{2} \frac{R_2}{R_1} + \frac{R_4 (R_1 + R_2)}{R_1 (R_3 + R_4)} v_{cm} + v_{cm} \frac{R_4 R_1 - R_2 R_3}{R_1 (R_3 + R_4)} \\ G_d &= \frac{1}{2} \frac{R_2}{R_1} + \frac{R_4 (R_1 + R_2)}{R_1 (R_3 + R_4)} & G_{cm} &= \frac{R_4 R_1 - R_2 R_3}{R_1 (R_3 + R_4)} \\ CMRR &= 20 \log \left| \frac{G_d}{G_{cm}} \right| = 20 \log \left| \frac{1}{2} \frac{R_2 (R_3 + R_4) + R_4 (R_1 + R_2)}{R_4 R_1 - R_2 R_3} \right| \end{aligned}$$

3. (Prudent time allocation = 30 minutes)

Consider an npn BJT with the following  $I_C$ - $V_{CE}$  characteristic:



Suppose that such a transistor is used in the circuit illustrated below.



- a. By drawing a **load line** on the characteristic curve, choose the circuit **quiescent point** or DC operating point to maximize the AC voltage swing of  $V_{out}(t)$ . What are the DC values of the bias current, the collector current,  $R_B$  and  $V_{out}$  at the quiescent point (carefully specify units)?

$$\text{DC bias current} = 3.5 \mu\text{A}$$

$$\text{DC collector current} = 0.39 \text{ mA}$$

$$\text{DC output voltage} = 3.2 \text{ V}$$

$$\text{Bias resistor} = (7.0 - 0.7)/3.5 \times 10^{-6} = 1.8 \text{ M}$$

- b. For these quiescent point values, sketch in the space on the next page a **complete small-signal equivalent circuit** of the transistor including values and units for all parameters of the equivalent circuit (neglect any high frequency effects).

From the graph at the Q - point:

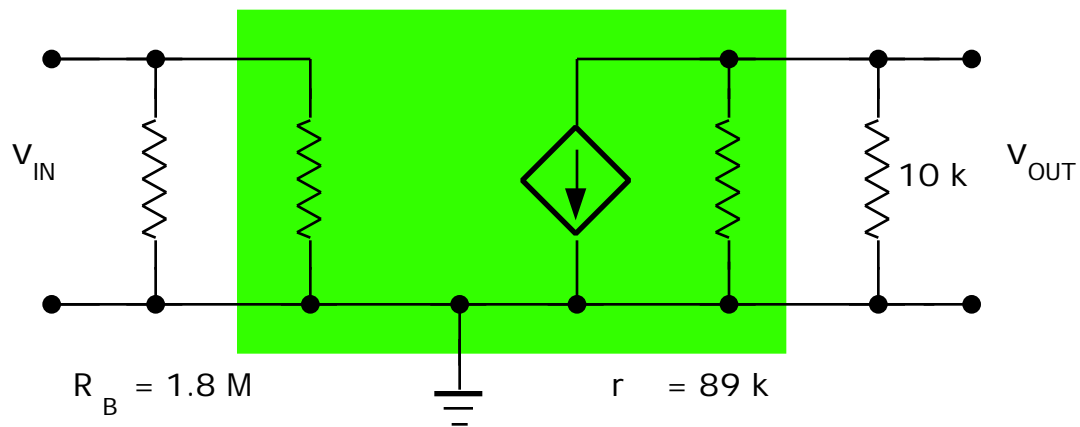
$$= \frac{0.33 \text{ mA}}{3 \mu\text{A}} \cdot 110$$

$$g_m = \frac{I_c}{V_T} = \frac{0.39 \text{ mA}}{25 \text{ mV}} = 0.016 \text{ }^{-1}$$

$$r = \frac{110}{g_m} = \frac{110}{0.016 \text{ }^{-1}} = 6.9 \text{ k}$$

$$r_o = \frac{V_{cc}}{i_c} = \frac{8 \text{ V}}{0.09 \text{ mA}} = 89 \text{ k}$$

$$r = 6.9 \text{ k} \quad g_m v = (0.016 \text{ }^{-1}) v$$



- c. Again at the quiescent point found above and at frequencies where we can neglect capacitive effects, find the small-signal voltage gain, input impedance and output impedance of the circuit.

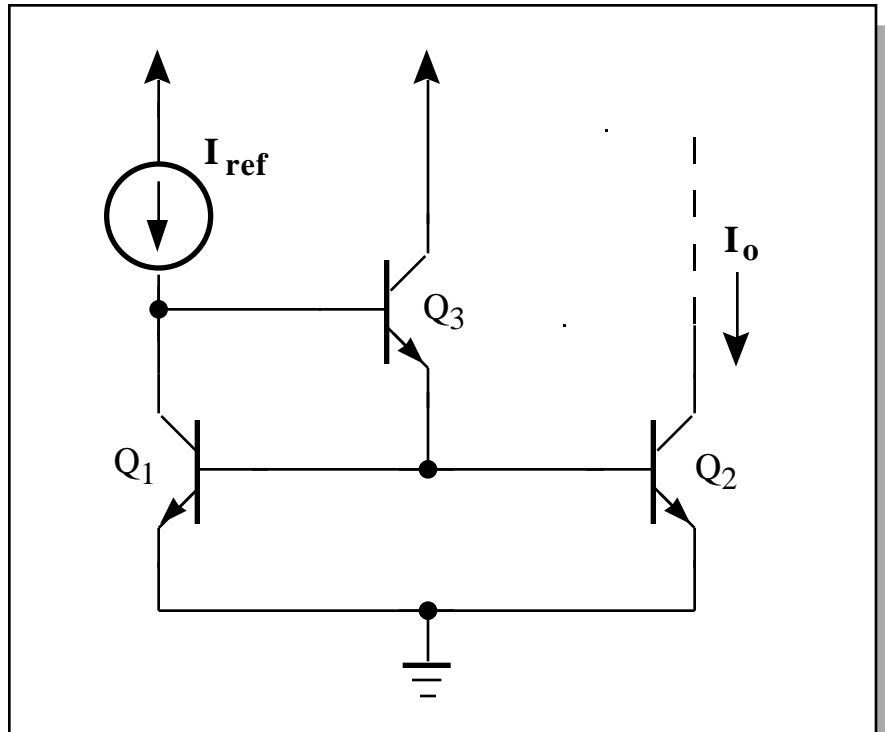
$$\text{Small-signal voltage gain} = (0.016 \text{ }^{-1}) (89 \parallel 10) \text{ k} = 144$$

$$\text{Small-signal input impedance} = 1.8 \text{ M} \parallel 6.9 \text{ k} = 6.9 \text{ k}$$

$$\text{Small-signal output impedance} = (89 \parallel 10) \text{ k} = 9.0 \text{ k}$$

**4. (Prudent time allocation = 15 minutes)**

If in the following circuit we assume that the three transistors are identical, find an expression for the ratio  $I_o/I_{ref}$  in terms of the  $\beta$  of the transistors.

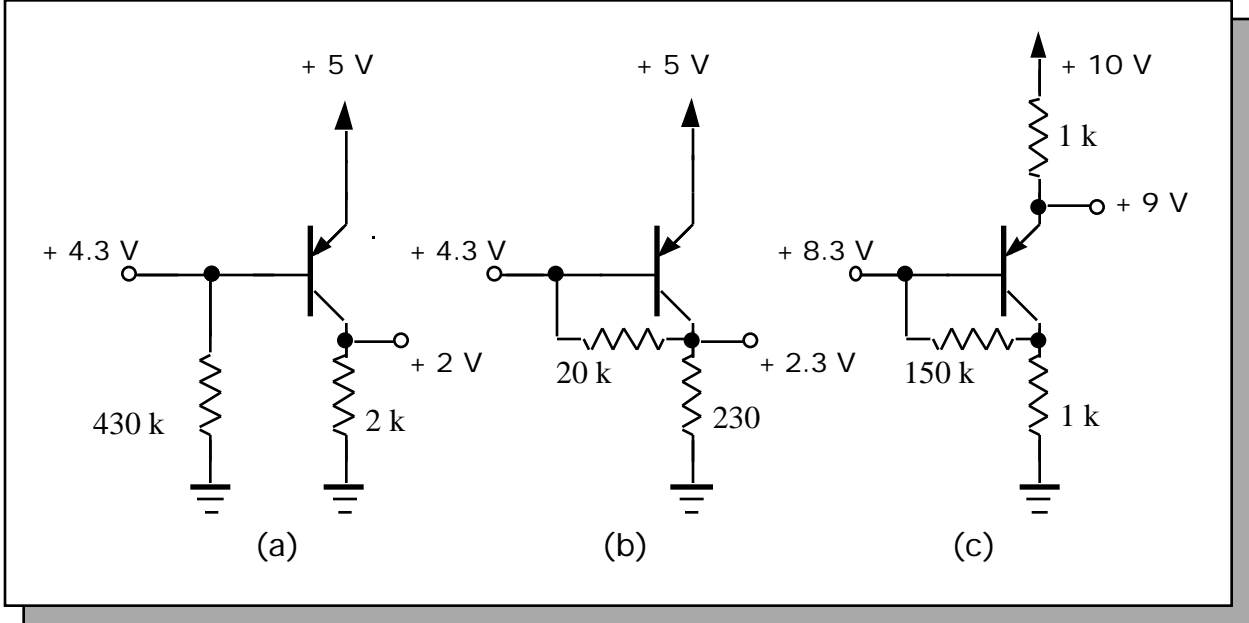


**See the discussion at:**

[www.deas.harvard.edu/courses/es154/lectures/lecture\\_6/mirrors/mirrors.html#base\\_comp](http://www.deas.harvard.edu/courses/es154/lectures/lecture_6/mirrors/mirrors.html#base_comp)

5. (Prudent time allocation = 10 minutes)

Measurements on the three circuits below yield the voltages indicated. Find the value of  $\beta$  for each of the pnp transistors.



(a) =

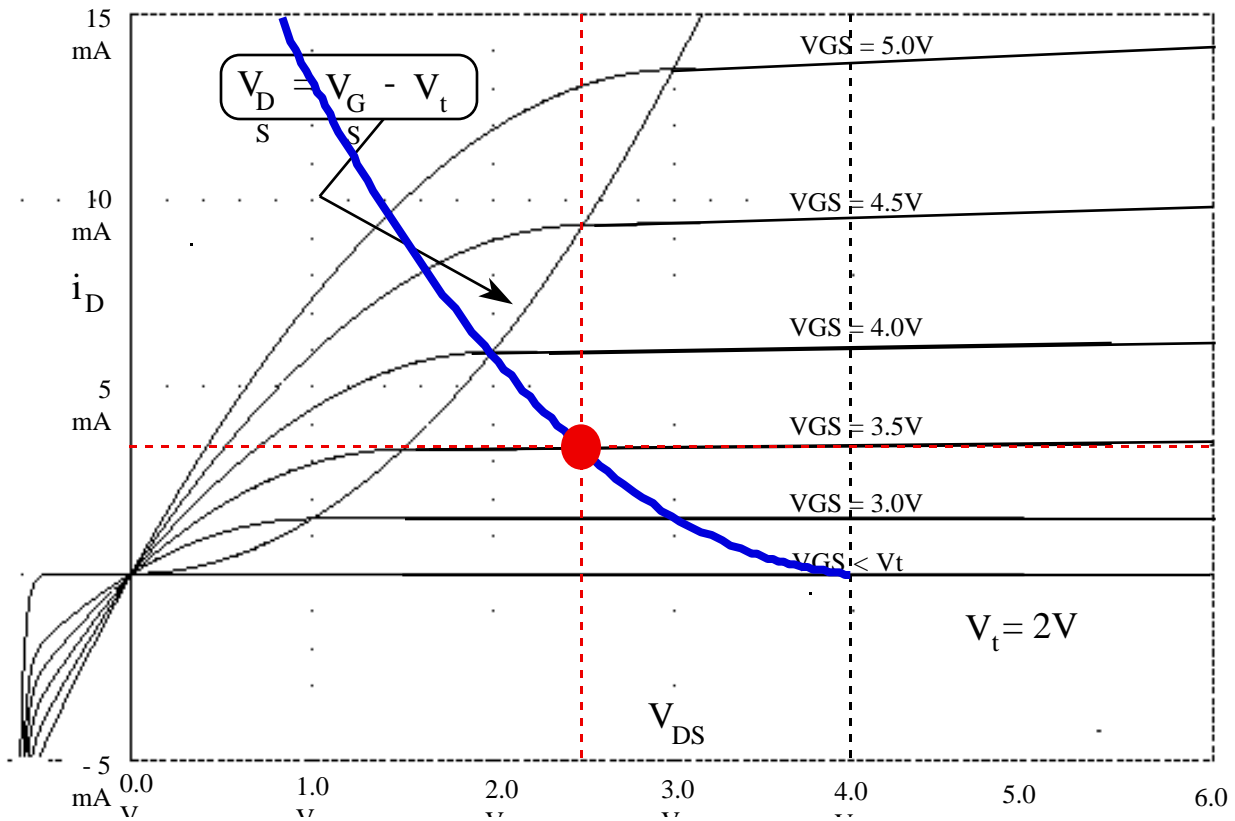
(b) =

(c) =

6. (Prudent time allocation = 20 minutes)

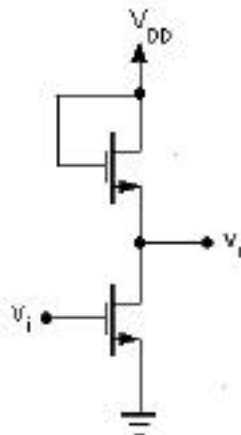
Consider a NMOS enhancement transistor with the following characteristics:

Output Characteristics of a 2N6762 NMOS Enhancement Transistor



Suppose two such transistors are used in a common source, NMOS amplifier configuration where one transistor serves as the load of the other . Assume that the amplifier is powered by a single-sided + 6 volt supply.

a. Draw a circuit of such an enhancement loaded amplifier in the space below:



- b. Draw directly on the characteristic curve above the appropriate **load curve** for the amplifier. **See characteristic curve**
- c. Using this load curve, choose a **quiescent point** or **dc operating point** so as to maximize the ac voltage swing of the amplifier output. What are the dc values of the bias voltage, the drain current, and the drain-source voltage at the quiescent point (carefully specify units)?

**dc bias voltage = 3.5 V**

**dc drain current = 3 mA**

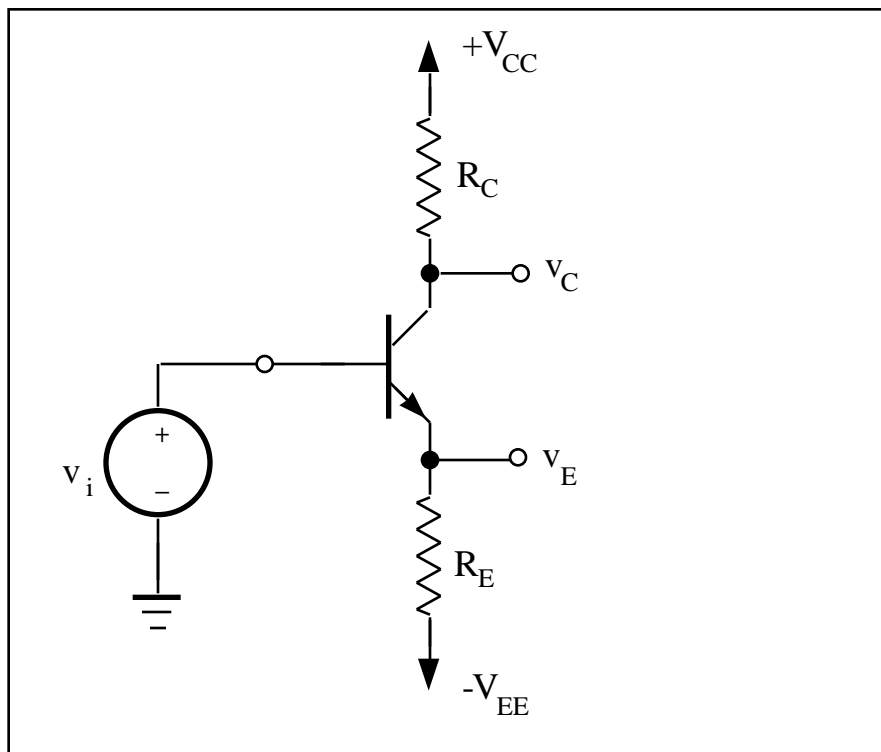
**dc drain-source voltage = 2.5 V**

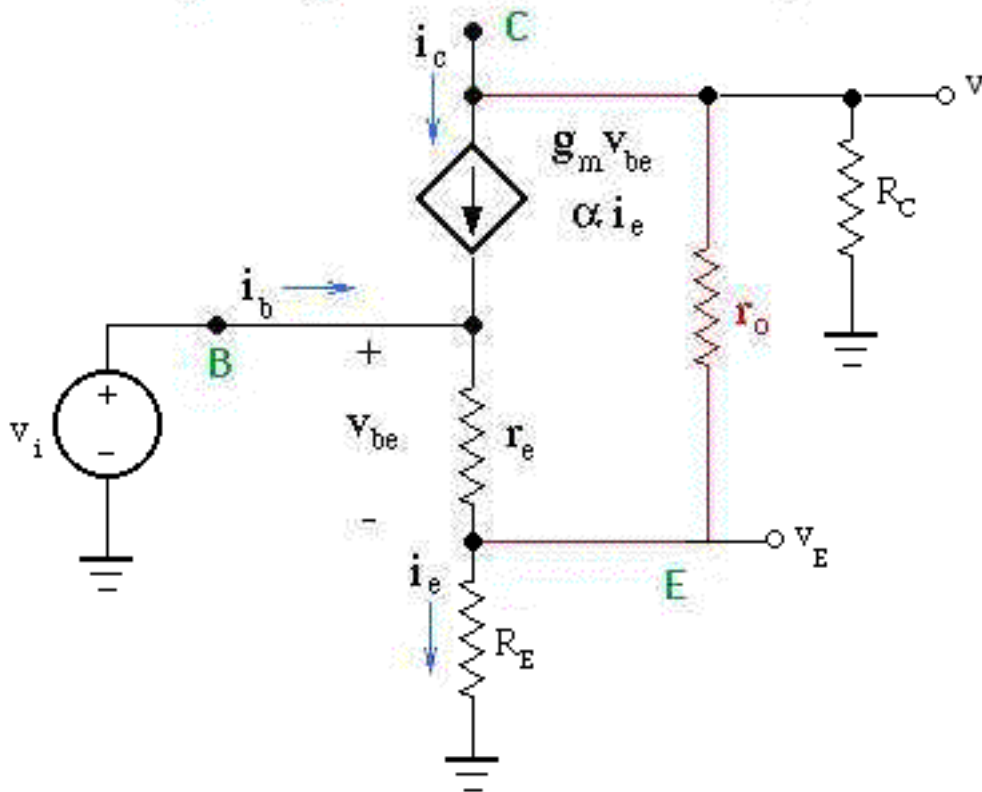
- d. For these quiescent point values, find the ac voltage gain of the amplifier.

**voltage gain 1**

**7. (Prudent time allocation = 15 minutes)**

As the first step in analyzing the following BJT amplifier, replace the transistor with its low-frequency “T” equivalent circuit. Then, derive the gain  $v_E/v_i$ , the gain  $v_C/v_i$ , and the input impedance of the amplifier.





Nodal Analysis (neglecting  $r_o$  - i.e  $r_o$  ):

Node B

$$i_b + g_m (v_i - v_E) + \frac{v_E}{r_e} = \frac{v_i}{r_e}$$

Node C

$$g_m (v_i - v_E) + \frac{v_C}{R_C} = 0$$

Node E

$$\frac{v_E}{r_e \parallel R_E} = \frac{v_i}{r_e}$$

Nodal Analysis (including  $r_o$ ):

Node B

$$i_b + g_m (v_i - v_E) + \frac{v_E}{r_e} = \frac{v_i}{r_e}$$

Node C

$$g_m (v_i - v_E) + \frac{v_C}{r_o \parallel R_C} = \frac{v_E}{r_o}$$

Node E

$$\frac{v_E}{r_o} + \frac{v_E}{r_e \parallel R_E} = \frac{v_C}{r_o} + \frac{v_i}{r_e}$$

Results (neglecting  $r_o$  - i.e  $r_o$  ):

$$\frac{v_E}{v_i} = \frac{r_e \parallel R_E}{r_e} = \frac{R_E}{r_e + R_E}$$

$$\frac{v_C}{v_i} = -g_m R_C \frac{r_e}{r_e + R_E}$$

$$\frac{1}{R_{in}} = \frac{i_b}{v_i} = - \frac{r_e}{r_e + R_E} g_m - \frac{1}{r_e}$$

Results (including  $r_o$ ):

$$\frac{v_E}{v_i} = \frac{\frac{r_e \parallel R_E}{r_e} - g_m \frac{r_o \parallel R_C}{r_o} (r_e \parallel R_E)}{1 - g_m \frac{r_o \parallel R_C}{r_o} (r_e \parallel R_E) + \frac{r_o \parallel R_C}{r_o R_C} (r_e \parallel R_E)}$$

$$\frac{v_C}{v_i} = \frac{-g_m (r_o \parallel R_C) \frac{r_e \parallel R_E}{r_o} \left(1 + \frac{r_o}{R_E} + \frac{r_e \parallel R_E}{r_e} \frac{r_o \parallel R_C}{r_o}\right)}{1 - g_m \frac{r_o \parallel R_C}{r_o} (r_e \parallel R_E) + \frac{r_o \parallel R_C}{r_o R_C} (r_e \parallel R_E)} \quad s$$

$$\frac{1}{R_{in}} = \frac{i_b}{v_i} = - \frac{\frac{r_e \parallel R_E}{R_E} + \frac{r_o \parallel R_C}{r_o R_C} (r_e \parallel R_E)}{1 - g_m \frac{r_o \parallel R_C}{r_o} (r_e \parallel R_E) + \frac{r_o \parallel R_C}{r_o R_C} (r_e \parallel R_E)} \quad g_m - \frac{1}{r_e}$$

**8. (Prudent time allocation = 10 minutes)**

For a particular npn transistor operating in the active mode the collector current is measured to be 1 mA and 10 mA for base-to-emitter voltages of 0.63 V and 0.70 V, respectively. Find the corresponding values of  $n$  and  $I_S$  for this transistor.

Assume that  $I_C(V_{BE}) = I_S \exp \frac{V_{BE}}{n V_T}$

therefore  $n = \frac{1}{V_T} \frac{(V_1 - V_2)}{\ln \frac{I(V_1)}{I(V_2)}} = \frac{1}{25 \text{ mV}} \frac{(0.7 - 0.63) \text{ V}}{\ln \frac{10}{1}} = \frac{70 \text{ mV}}{25 \text{ mV}} \frac{1}{2.3} = 1.2$

and  $I_S = \frac{I_C(V_{BE})}{\exp \frac{V_{BE}}{n V_T}} = \frac{10 \text{ mA}}{\exp \frac{700 \text{ mV}}{30 \text{ mV}}} = \frac{10 \text{ mA}}{1.36 \times 10^{10}} = 0.74 \times 10^{-12} \text{ A}$

- a. If two such devices are connected in parallel and a forward bias of 0.65 V is applied across the two base-emitter junctions, what total collector current do you expect?

$$I_C(650 \text{ mV}) = 2 \times (0.74 \times 10^{-12} \text{ A}) \exp \frac{650 \text{ mV}}{30 \text{ mV}} = 3.8 \text{ mA}$$

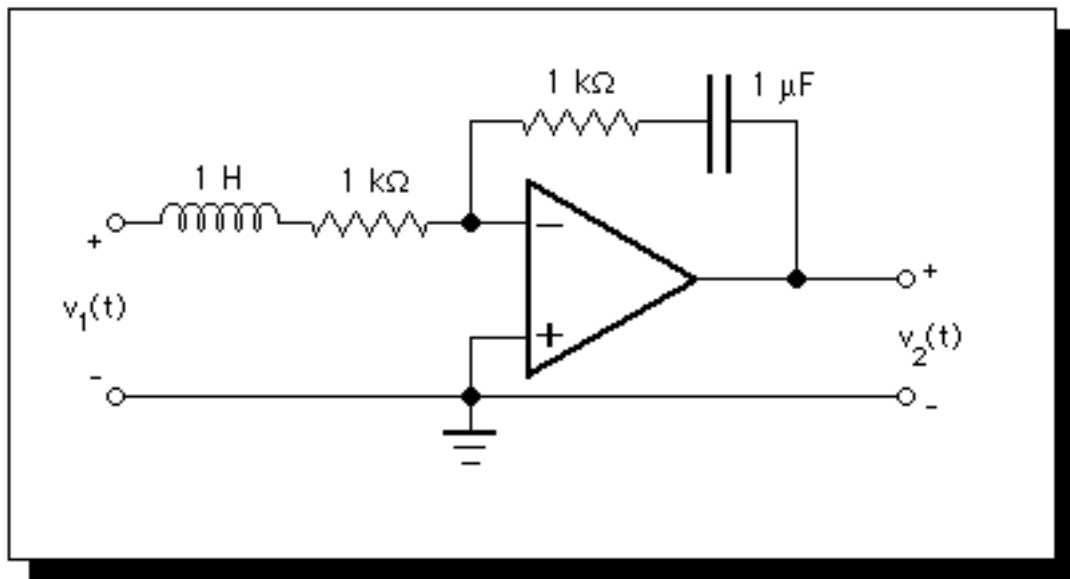
9. (Prudent time allocation = 12 minutes)

- Draw a complete circuit diagram of an emitter-follower amplifier which uses an npn BJT.
- Draw a small-signal version of this complete emitter-follower that utilizes the most appropriate BJT small-signal equivalent circuit.
- Using this small-signal circuit, find an expression for the voltage gain of the amplifier
- Again using this small-signal circuit, find an expression for the input impedance of the amplifier.

See discussion at:

[www.deas.harvard.edu/courses/es154/lectures/lecture\\_3/bjt\\_amps/bjt\\_amps.html#ce\\_amp](http://www.deas.harvard.edu/courses/es154/lectures/lecture_3/bjt_amps/bjt_amps.html#ce_amp)

10. (Prudent time allocation = 10 minutes)



- Assuming that the op amp is *ideal*, find the transfer function  $H(s) = V_2(s)/V_1(s)$ .

$$\frac{V_1(s)}{10^3 + s} = \frac{-V_2(s)}{10^3 + \frac{10^6}{s}}$$

$$H(s) = \frac{V_2(s)}{V_1(s)} = -\frac{10^3 + \frac{10^6}{s}}{10^3 + s} = -\frac{1 + \frac{10^3}{s}}{1 + \frac{s}{10^3}}$$

- b. Describe the behavior of this transfer function in both the high and low frequency limits.

$$H(s) = \frac{V_2(s)}{V_1(s)} \quad \begin{matrix} -\frac{10^3}{s} & 0 \\ 0 & -\frac{10^3}{s} \end{matrix}$$

**11. (Prudent time allocation = 15 minutes)**

- Draw a complete circuit diagram of an source-follower amplifier which uses an n-channel MOSFET.
- Draw a small-signal version of this complete source-follower that utilizes the most appropriate MOSFET small-signal equivalent circuit.
- Using this small-signal circuit, find an expression for the voltage gain of the amplifier
- Again using this small-signal circuit, find an expression for the input impedance of the amplifier.

**See and adapt the “The Common-Collector Amplifier or Emitter Follower” discussion on page 290-295 in Sedra & Smith.**