EE 560
FABRICATION OF MOS CIRCUITS

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CMOS CHIP MANUFACTURING STEPS

Substrate Wafer → **Wafer Fabrication** (diffusion, oxidation, photomasking, ion implantation, thin film deposition, etc.) → Finished Wafer

Wafer Probe Tests

Finished Wafer → **Final Tests**

**Finished Integrated Circuits**

**Wafer Fabrication**

**Packaging** (encapsulation) → **Visual Inspection** → **Chip Separation**
CMOS PROCESSING TECHNOLOGY

DIFFUSION PROCESS

Boron atoms deposited on surface

High Temp Treatment (> 800°C)

Impurity Concent - atoms/cm³

Depth x - μm

- Boron typically used for p-type doping
- Arsenic and Phosphorus are typically used for n-type doping.

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Methods for inserting impurity atoms into Si substrate

- Diffusion (high temperature)
- Epitaxial growth followed by diffusion
- Ion implantation (high velocity)
Local Oxidation of Silicon (LOCOS)

-> Fabricate thin SiO$_2$ layer adjacent to THICK SiO$_2$ layers.

-> Transition from THICK to thin SiO$_2$ layers fabricated WITHOUT creating sharp vertical transitions.

SiN acts as barrier to oxygen atoms, stops further oxidation at SiN-SiO$_2$ interface.
A FABRICATED n-MOS TRANSISTOR

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Simplified process sequence for the fabrication of an n-well CMOS IC with a single polysilicon layer:

1. Create n-well regions & channel stop regions.
2. Grow field oxide (thick oxide) & gate oxide (thin oxide).
3. Deposit & pattern polysilicon layer.
4. Implant source & drain regions, substrate contacts.
5. Create contact windows, deposit & pattern metal layer.
Fabrication Steps in Si-Gate NMOS Process

1. **Patterning SiO₂ Layer**
   - SiO₂
   - p-substrate

2. **Gate Oxidation**
   - Thin Oxide
   - 100A - 300A
   - p-substrate

3. **Patterning Polysilicon**
   - Polysilicon
   - 0.5 µm - 2 µm
   - p-substrate

4. **Source, Drain Inplants or Diffusions (self aligned)**
   - implant of impurities
   - ≈ 1 µm deep
   - p-substrate

5. **Contact Cuts**
   - SiO₂ by deposition
   - p-substrate

6. **Patterning Al Layer**
   - Aluminum contacts
   - p-substrate

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Parasite MOS Transistor
or Field Device

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Typical N-Well CMOS Process

Physical Structure

Mask Top View

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CMOS INVERTER LAYOUT IN AN N-WELL CMOS PROCESS

COLOR LEGEND
- Brown: n-Well
- Green: n⁺
- Red: Polysilicon
- Yellow: p⁺
- Dark gray: Gate Oxide
- Light gray: Field Oxide
- Light blue: Metal 1
- Orange: Metal 2
- Gray: Metal 3
- Black: Contact/via

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CMOS INVERTER IN TWIN-WELL CMOS PROCESS

COLOR LEGEND

- n-Well
- p-Well
- n^+
- Polysilicon
- p^+
- Gate Oxide
- Field Oxide
- Metal 1
- Metal 2
- Metal 3
- Contact/via
CMOS PROCESS ENHANCEMENTS

1. INTERCONNECT
   A. Metal Interconnect (two, three, four or more levels)
   B. Polysilicon (two or more levels, also for high quality capacitors)
   C. Polysilicon/Refractory Metal Interconnect
   D. Local Interconnect

2. CIRCUIT ELEMENTS
   A. Resistors
   B. Capacitors
   C. Electrically Alterable ROM (EAROM - EEROM - EEPROM)
   D. Bipolar Transistors
COLOR LEGEND
- n-Well
- n⁺
- Polysilicon
- p⁺
- Gate Oxide
- Field Oxide
- Metal 1
- Metal 2
- Metal 3
- Contact/via

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Polysilicon/Refractory Metal or Silicide Gate/Interconnect Structures

Silicide Gate (e.g. silicon and tantalum)

Doped Polysilicon: $R_{\text{sheet}} = 20$ to $40 \ \Omega/\text{Square}$

Silicide: $R_{\text{sheet}} = 1$ to $5 \ \Omega/\text{Square}$

Polysilicon/Silicide (Polycide) Gate
Self-Aligned Polysilicon/Silicide (Salicide)

(i) Polysilicon/silicide gate,

(ii) Silicide source/drain(s)
CMOS DOUBLE POLY CAPACITORS

Poly 1 → Poly 2

Capacitor SiO₂ layer (100 - 200 Å)

\[ C = C_{oxC} \cdot WL \]

\[ C_{oxC} = \frac{\varepsilon_{ox}}{t_{oxC}} \]

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RESISTORS

\[ R = \left( \frac{\rho}{t} \right) \frac{L}{W} = R_s \frac{L}{W} \Omega \]

- \( \rho \) = resistivity
- \( t \) = thickness
- \( L \) = conductor length
- \( W \) = conductor width
- \( R_s \) = sheet resistance \( \Omega / \text{sq} \)

Typical Sheet Resistance for Conductors (\( R_s - \Omega / \text{sq} \))

<table>
<thead>
<tr>
<th>Material</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Metal - Meal 2</td>
<td>0.05</td>
<td>0.07</td>
<td>0.1</td>
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<tr>
<td>Metal 3</td>
<td>0.03</td>
<td>0.04</td>
<td>0.05</td>
</tr>
<tr>
<td>Polysilicon</td>
<td>15</td>
<td>20</td>
<td>30</td>
</tr>
<tr>
<td>Silicide</td>
<td>2</td>
<td>3</td>
<td>6</td>
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<tr>
<td>( n^+, p^+ ) Diffusion</td>
<td>10</td>
<td>25</td>
<td>100</td>
</tr>
<tr>
<td>n-Well</td>
<td>1K</td>
<td>2K</td>
<td>5K</td>
</tr>
</tbody>
</table>

\[ R_c = k \frac{L}{W} \Omega \]

\[ k = \frac{1}{\mu C_{ox} (V_{gs} - V_T)} \]

MOS Resistor

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EEPROM TECHNOLOGY

\[ I_{FN} = C_1 W L E_{ox}^2 e^{-E_0/E_{ox}} \]

where

\[ E_{ox} = \frac{V_{gs}}{t_{ox}} \]

electric field across tunnel oxide

\[ E_0 \text{ and } C_1 \text{ are process dependent constants} \]
BIPOLAR TRANSISTORS IN STANDARD CMOS

Substrate pnp Bipolar Transistor
PHYSICAL LAYER: prescription for preparing photomasks used in fabrication of ICs. Specify to the designer geometric constraints on the layout artwork so that patterns on the processed wafer will preserve the intended topology and geometry of the design.

PURPOSE: realize fabricated circuits optimum yield in smallest area possible without compromising the reliability of the circuit.

DESIGN RULE WAIVER: any significant and/or frequent departure from design rules.

TWO TYPES OF DESIGN RULES:
   a. line widths and separations
   b. interlayer registration

DESIGN RULE SPECS:
   a. 'micron' rules - minimum feature sizes and spacings in $\mu$m units (normal spec in industry)
   b. 'lambda ($\lambda$)' rules - minimum feature sizes and spacings speced in terms of a single parameter $\lambda$ (popularized by Mead and Conway and permits first order scaling)
The Design Process can be Abstracted to Manageable Number of Layout Levels that Represent the Physical Features on the Processed Silicon Wafer, i.e.

- Two different substrates (i.e. original substrate + well or twin wells)
- Doped regions p- and n- transistor forming materials (e.g. sources and drains)
- Transistor gate electrodes
- Interconnect paths
- Interlayer contacts
CMOS N-WELL DESIGN RULES

COLOR LEGEND
- n-Well
- p-Well
- n⁺
- Polysilicon
- p⁺
- Gate Oxide
- Field Oxide
- Metal 1
- Metal 2
- Metal 3
- Contact/via

\[ A1 = 10\lambda \]
\[ A2 = 6\lambda \]
\[ A2 = 8\lambda \]
\[ B1 = 3\lambda \]
\[ B2 = 3\lambda \]
\[ B3 = 5\lambda \]
\[ B4 = 3\lambda \]
\[ B5 = 5\lambda \]
\[ C1 = 2\lambda \]
\[ C2 = 2\lambda \]
\[ C3 = 1\lambda \]
\[ C4 = 3\lambda \]
\[ C5 = 2\lambda \]

Wells at the same potential
Wells at the different potential

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EFFECT OF INSUFFICIENT GATE EXTENSION

over-etched poly shrinks

diffusion bloats

source, drain short

gate extension (C4)

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EFFECT OF INSUFFICIENT SOURCE-DRAIN EXTENSION

mask misalignment changes width of device and sometimes completely eliminates it.

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TECHNOLOGY RELATED CAD ISSUES

TWO BASIC CHECKS MUST BE COMPLETED TO ENSURE THE MASK DATABASE DEVELOPED IN LAYOUT CAN BE TURNED INTO A WORKING CHIP:

a. To verify specified Design Rules have been obeyed  
   (DESIGN RULE CHECK or DRC)

b. To verify masks produce correct interconnected set of circuit elements  
   (MASK CIRCUIT-EXTRACTION)
TYPICAL DESIGN FLOW FOR THE PRODUCTION OF AN IC MASK SET

1. Functionality & performance specs
2. Circuit topology or schematic
3. Initial sizing of transistors
4. Estimate parasitic capacitances
5. Stick diagram layout
6. Mask layout design
7. Design Rule Check (DRC)
8. Circuit & parasitic extraction
9. Circuit simulation

Resize & Modify

Improve Performance

OK
Layout Complete