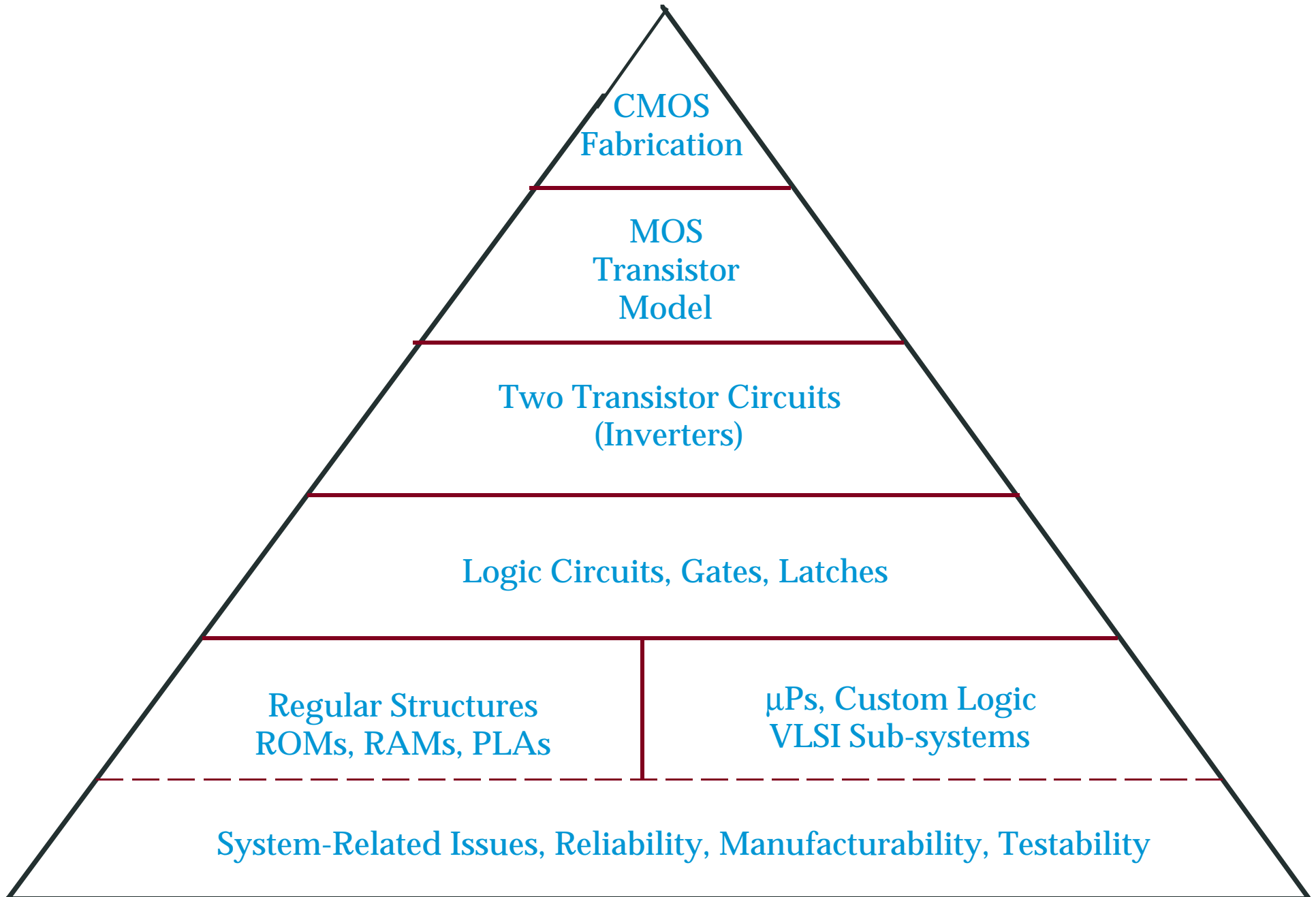


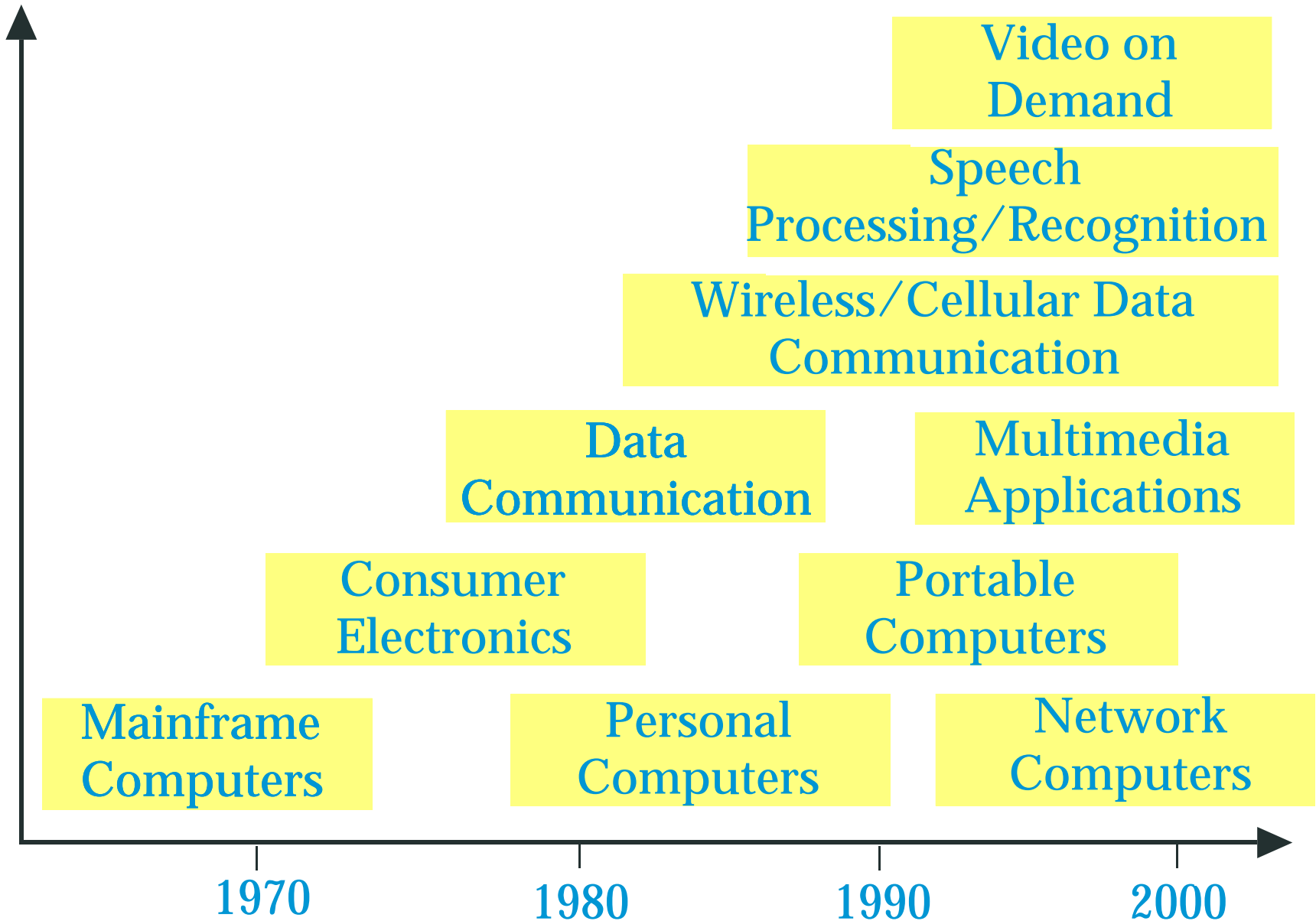
EE 560

INTRODUCTION

ORDERING OF TOPICS

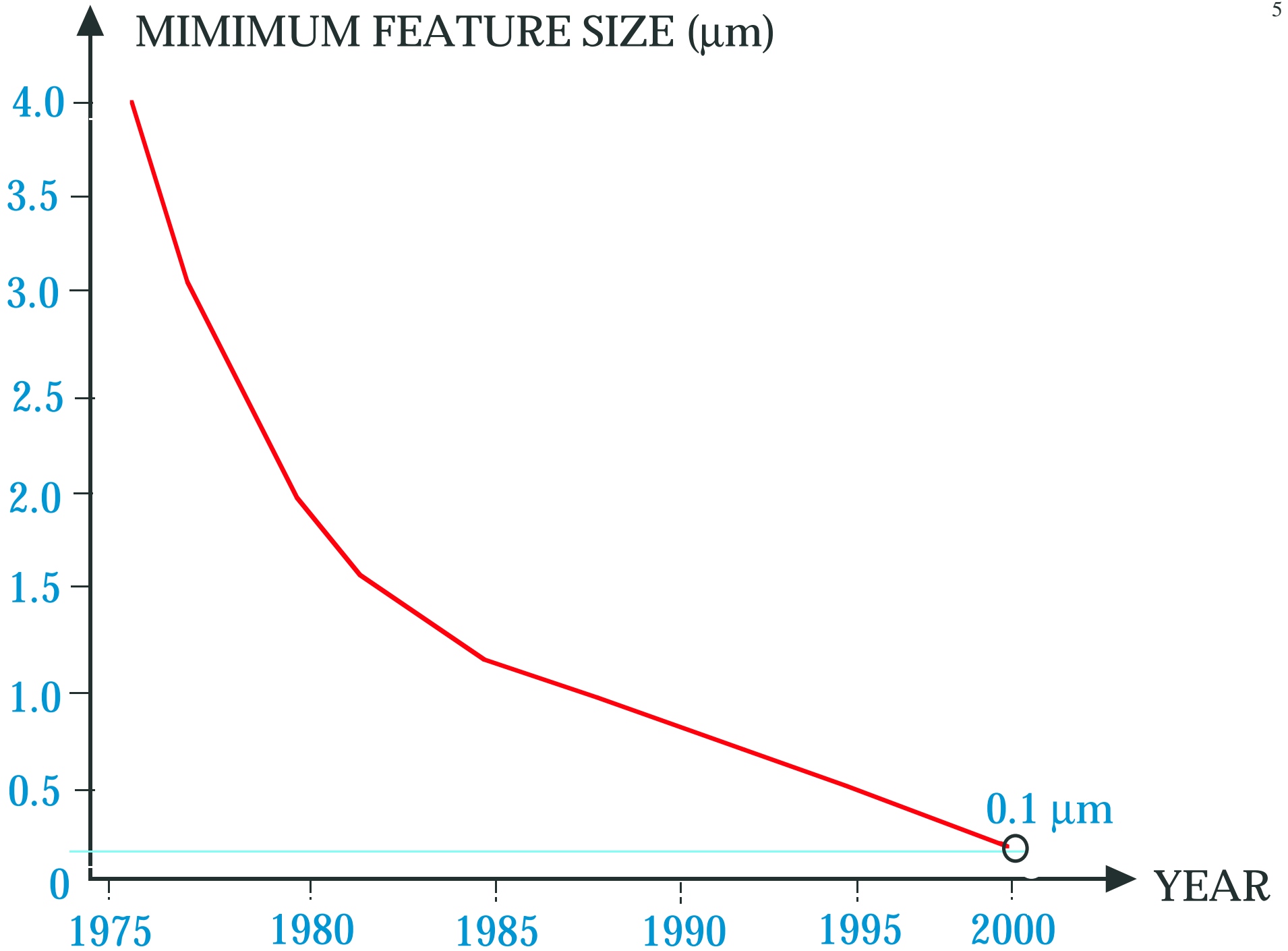


INFORMATION SERVICE INDUSTRY TRENDS



WHY MONOLITHIC INTEGRATION OF A LARGE NUMBER OF FUNCTIONS ON A SINGLE CHIP?

- Less die area, compactness
- Less power consumption
- Less testing requirements at the system level
- Higher reliability, due to high quality on chip interconnect
- Higher speed, due to reduced interconnect length
- Significant cost savings



CLASSIFICATION OF DIGITAL CIRCUIT TYPES 6

**DIGITAL
CIRCUITS**

```
graph TD; DC[DIGITAL CIRCUITS] --> S[STATIC CIRCUITS]; DC --> D[DYNAMIC CIRCUITS]; S --> CC[CLASSICAL CMOS]; S --> TGC[TRANSMISSION GATE CMOS]; S --> CV[CVSL CIRCUITS]; D --> DL[DOMINO LOGIC CIRCUITS]; D --> NL[NORA LOGIC CIRCUITS]; D --> TSPC[TSPC LOGIC CIRCUITS];
```

**STATIC
CIRCUITS**

**DYNAMIC
CIRCUITS**

**CLASSICAL
CMOS**

**TRANSMISSION
GATE CMOS**

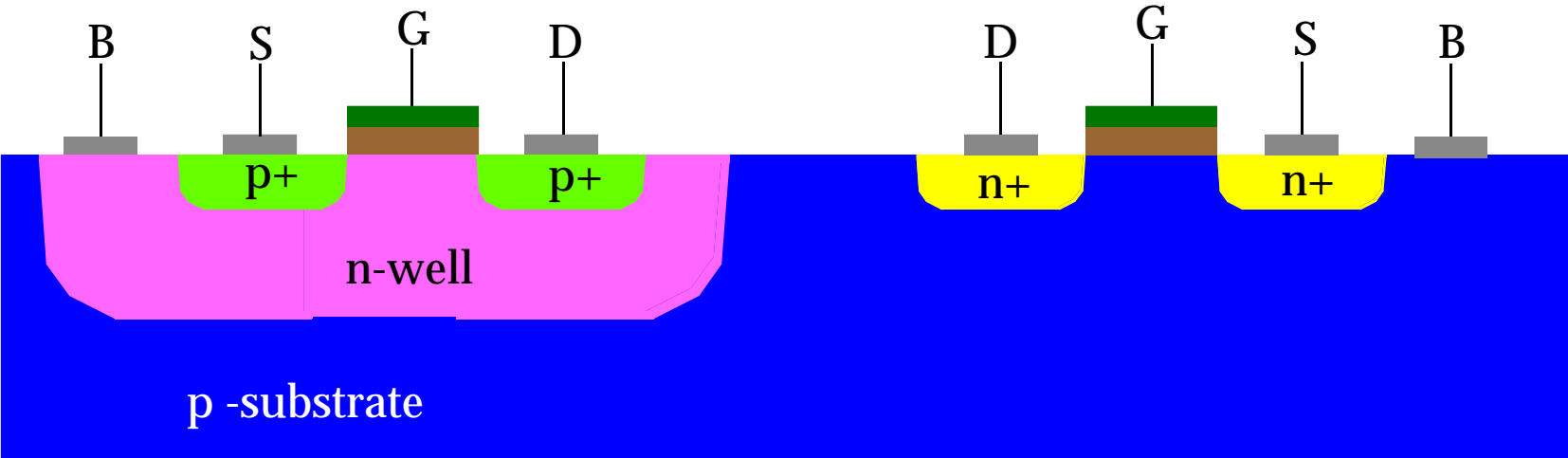
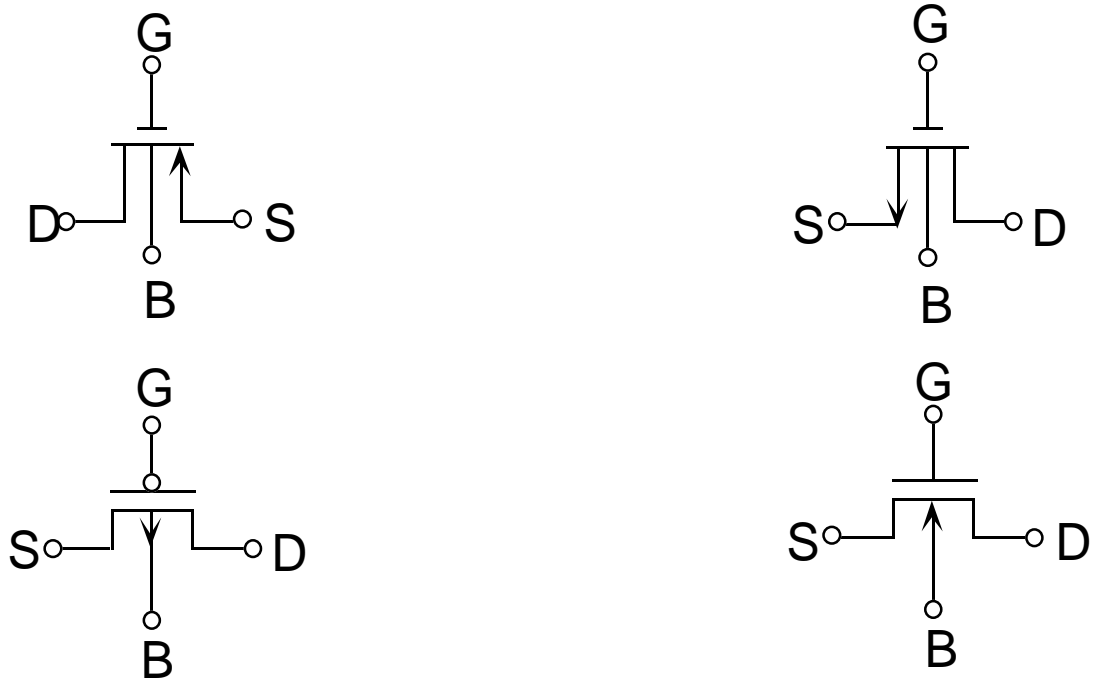
**CVSL
CIRCUITS**

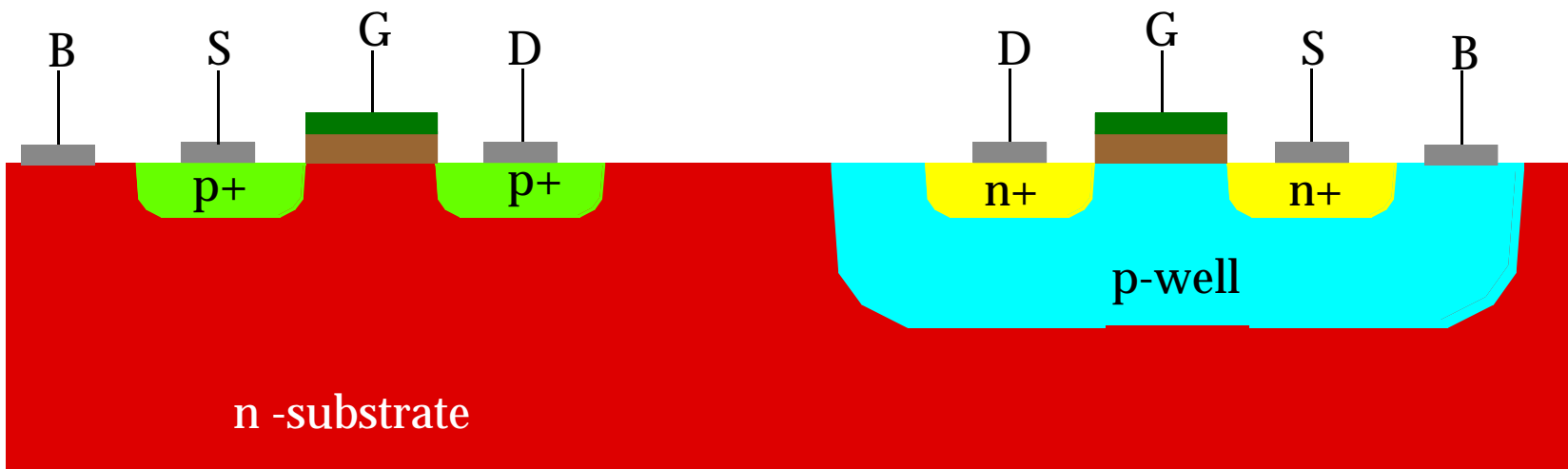
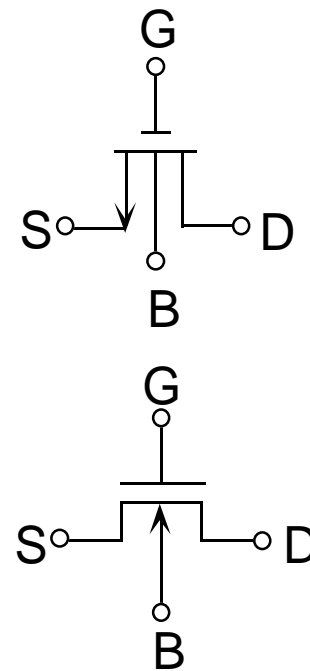
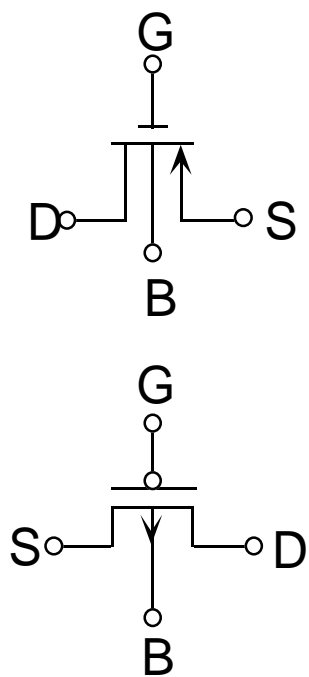
**DOMINO LOGIC
CIRCUITS**

**NORA LOGIC
CIRCUITS**

**TSPC LOGIC
CIRCUITS**

MOS TRANSISTORS



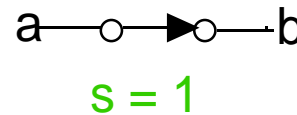
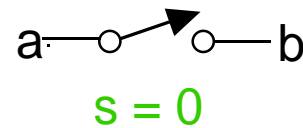
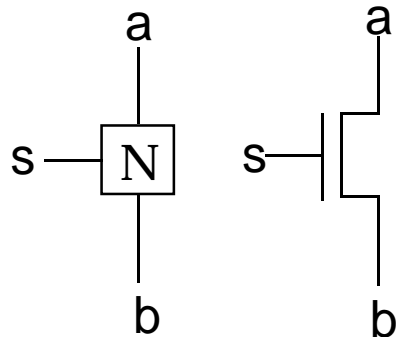


nMOS and pMOS SWITCH SYMBOLS AND IDEAL CHARACTERISTICS

SYMBOLS

SWITCH CHARACTERISTICS

N- SWITCH



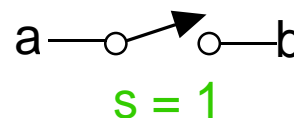
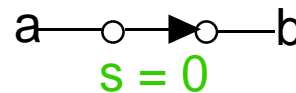
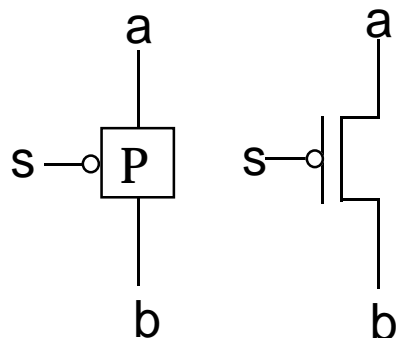
Input

Output

0 a — o — — o — b Strong 0

1 a — o — — o — b Weak 1

P- SWITCH



Input

Output

0 a — o — — o — b Weak 0

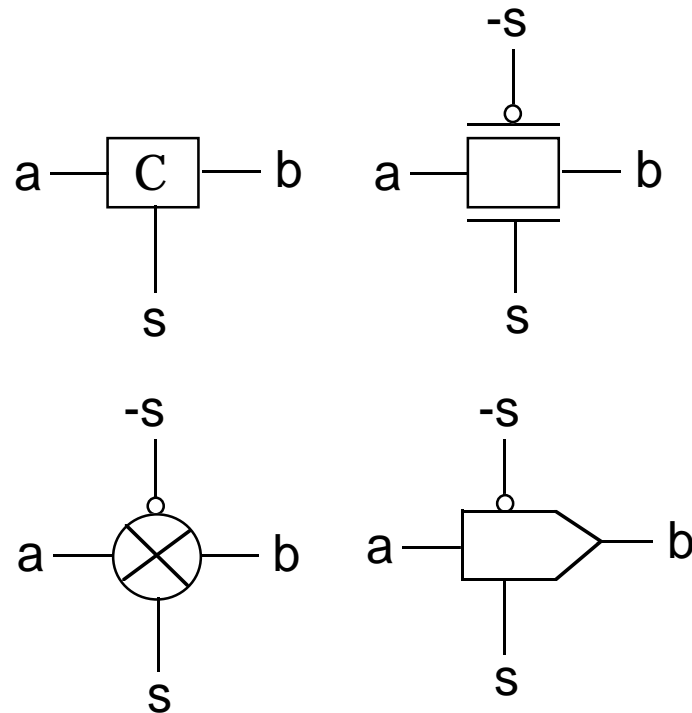
1 a — o — — o — b Strong 1

OUTPUT LOGIC LEVELS OF N- AND P- SWITCHES

LEVEL	SYMBOL	SWITCH CONDITION
Strong 1	1	P-SWITCH gate = 0, source = V_{DD}
Weak 1	1	N-SWITCH gate = 1, source = V_{DD}
Strong 0	0	N-SWITCH gate = 1, source = V_{SS}
Weak 0	0	P-SWITCH gate = 0, source = V_{SS}
High Impedance	Z	N-SWITCH gate = 0 or P-SWITCH gate = 1

COMPLEMENTARY CMOS SWITCH

SYMBOLS



SWITCH CHARACTERISTICS

Input

Output

0 a — o —▶— o — b Strong 0

1 a — o —▶— o — b Strong 1

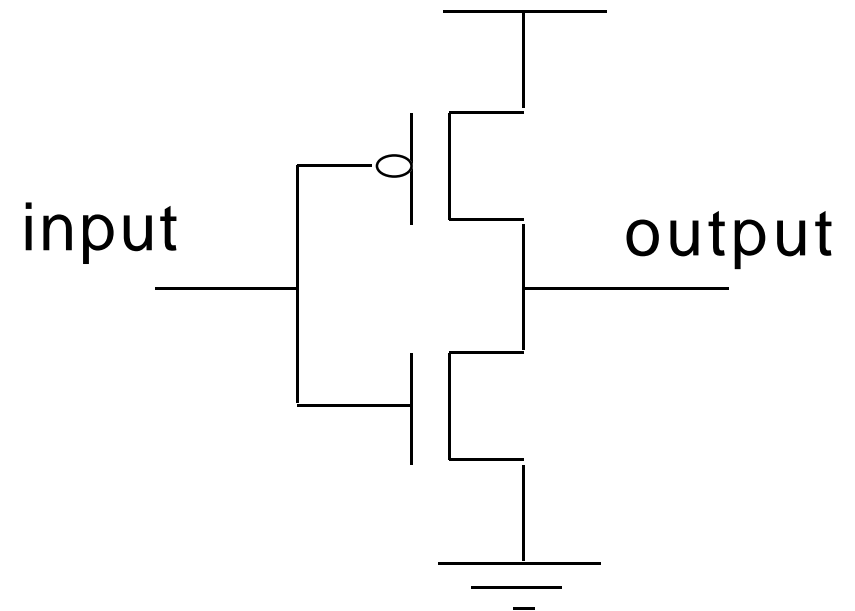
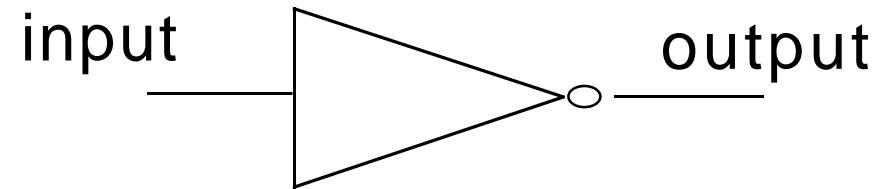
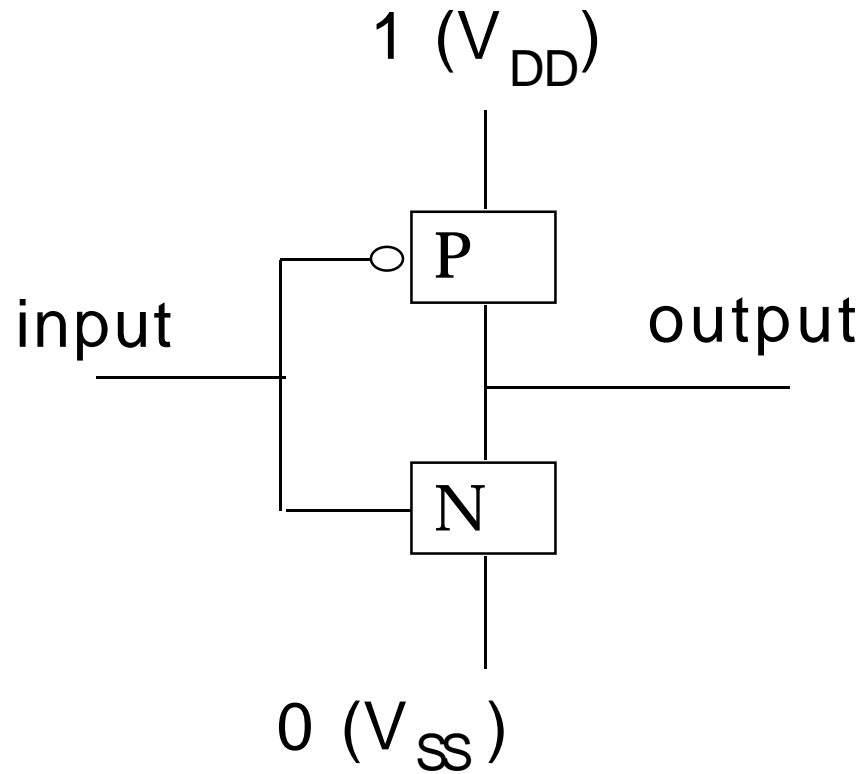
INVERTER TRUTH TABLE

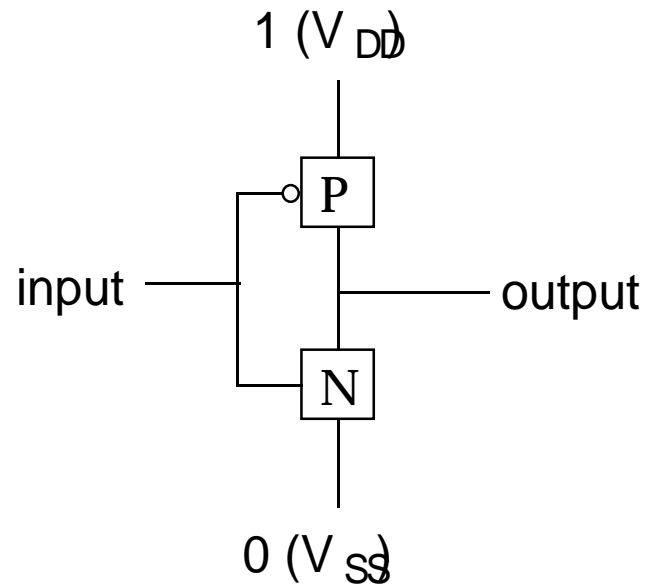
INPUT

0
1

OUTPUT

1
0





RESOLUTION OF GATE OUTPUT LEVELS

Pull-Down
Output

0
Z
Z
0

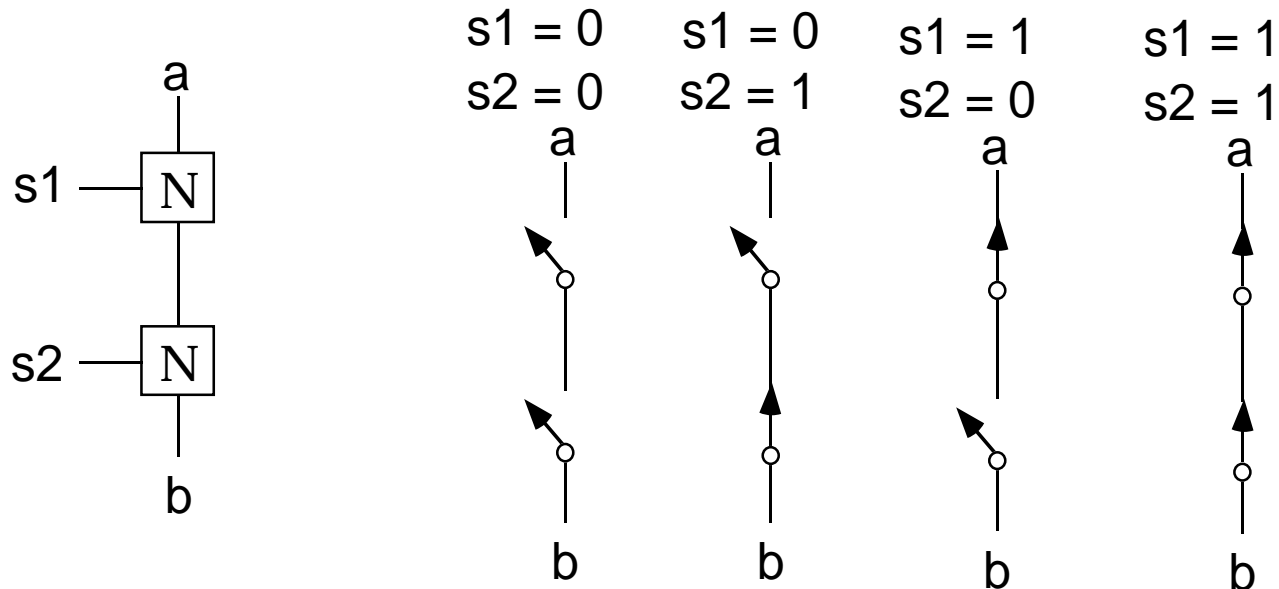
Pull-Up
Output

Z
1
Z
1

Combined
Output

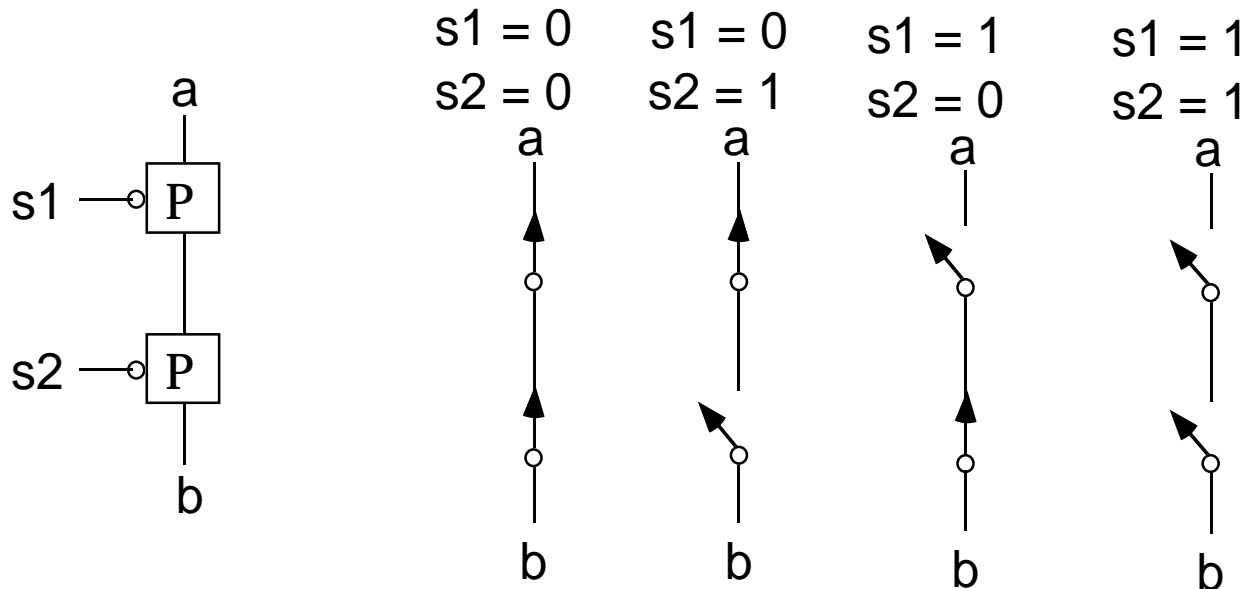
0
1
Z
CROSSBARRED

CONNECTION & BEHAVIOR OF SERIES N- AND P- SWITCHES



F

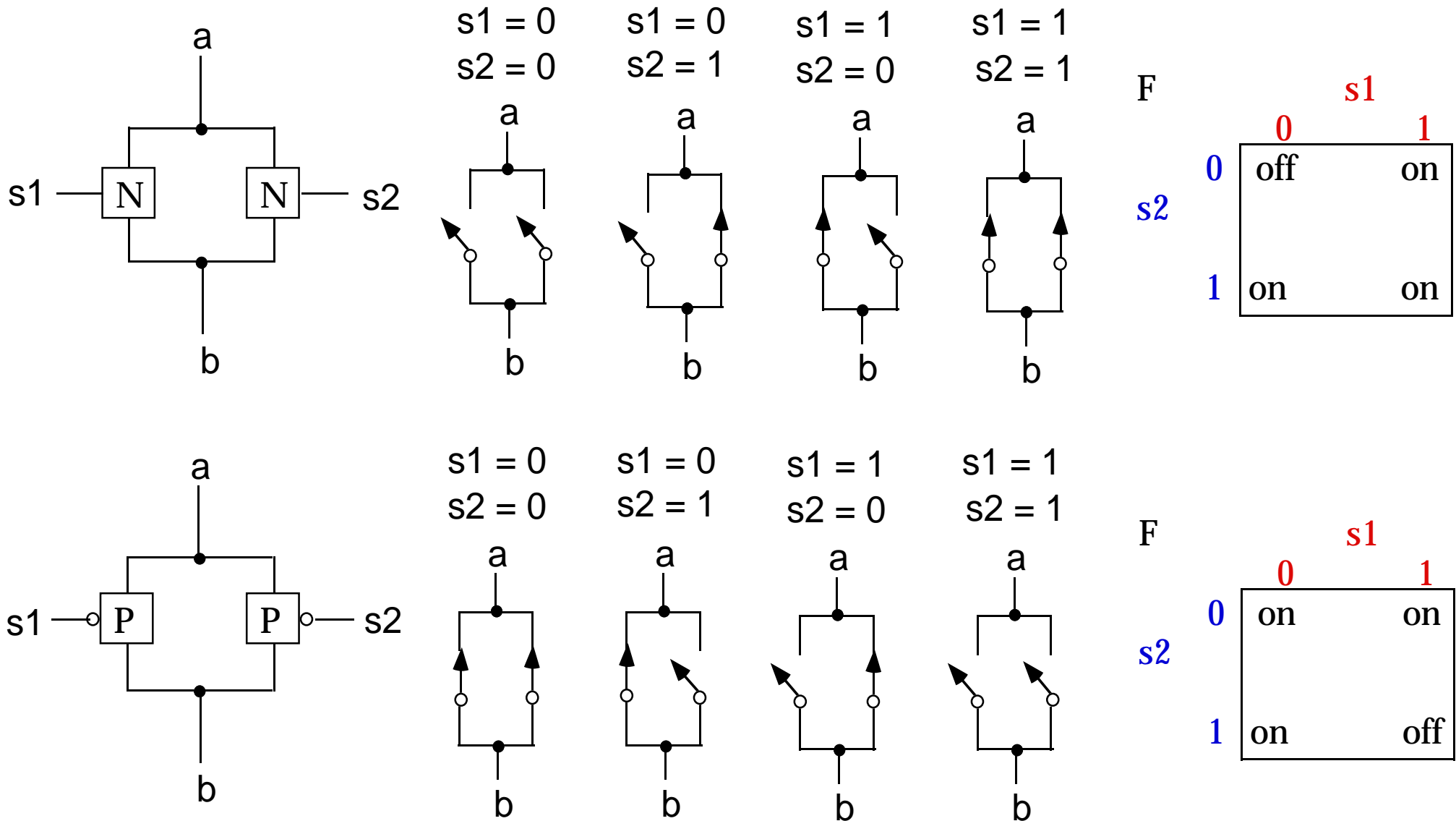
		s1	
		0	1
s2	0	off	off
	1	off	on



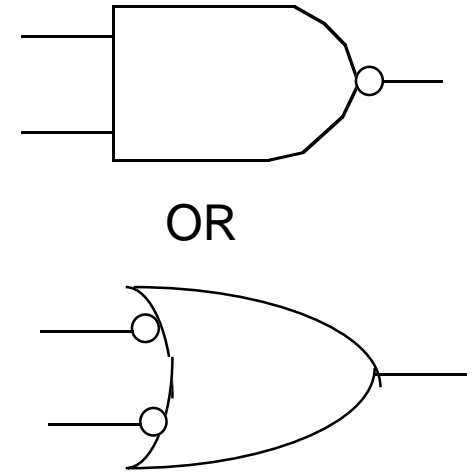
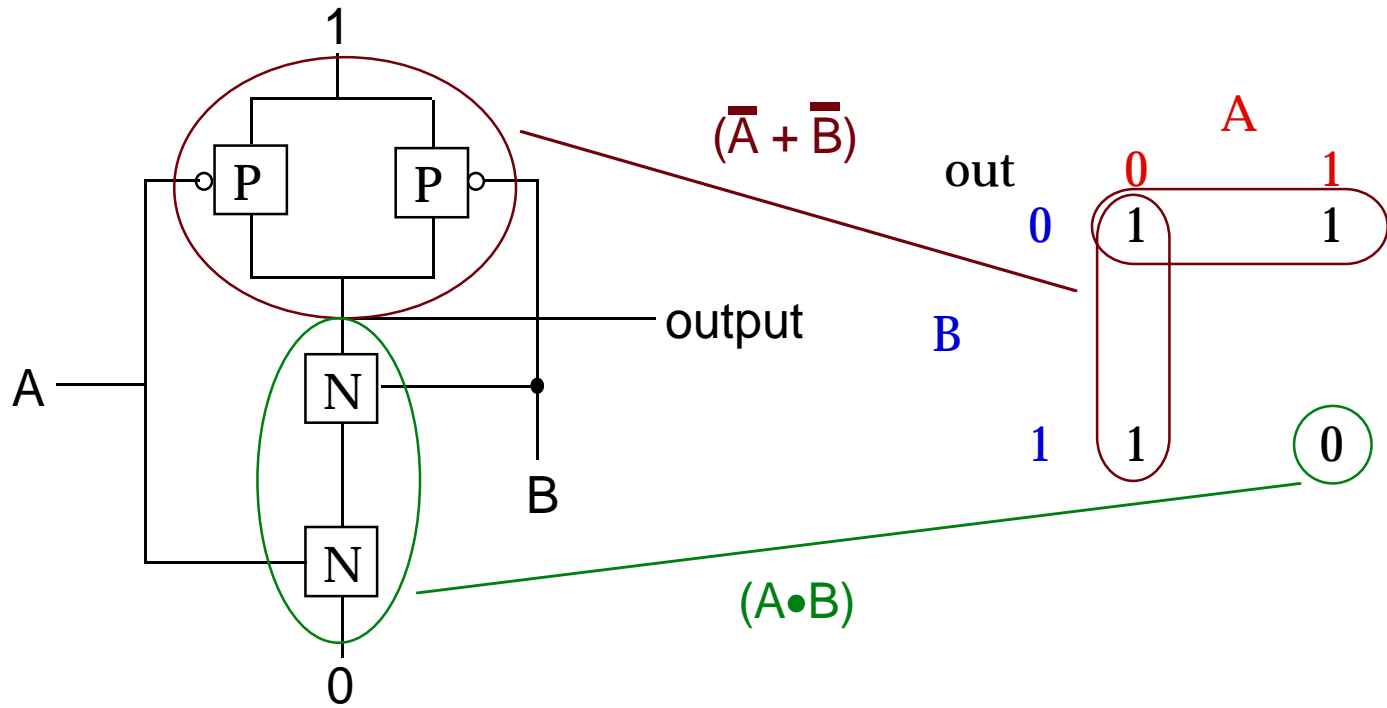
F

		s1	
		0	1
s2	0	on	off
	1	off	off

CONNECTION & BEHAVIOR OF PARALLEL N- AND P- SWITCHES



2-INPUT CMOS NAND GATE



2-INPUT CMOS NAND GATE TRUTH TABLE

OUTPUT

A-INPUT

0

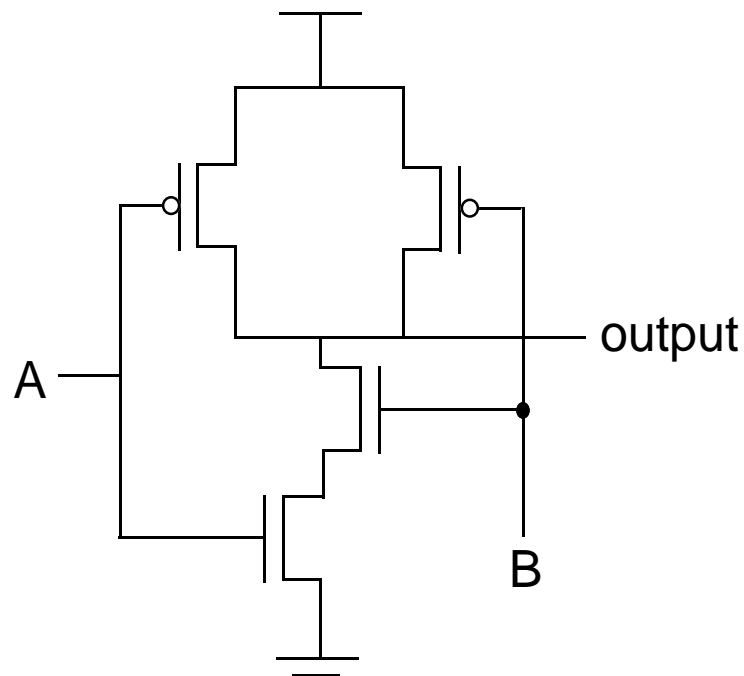
1

0

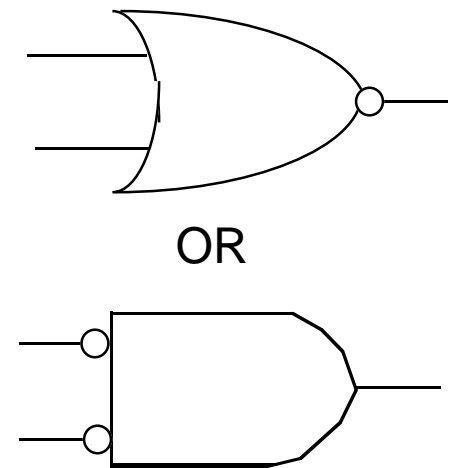
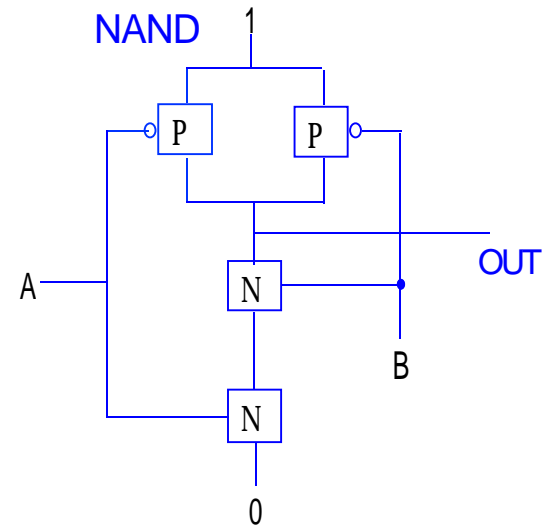
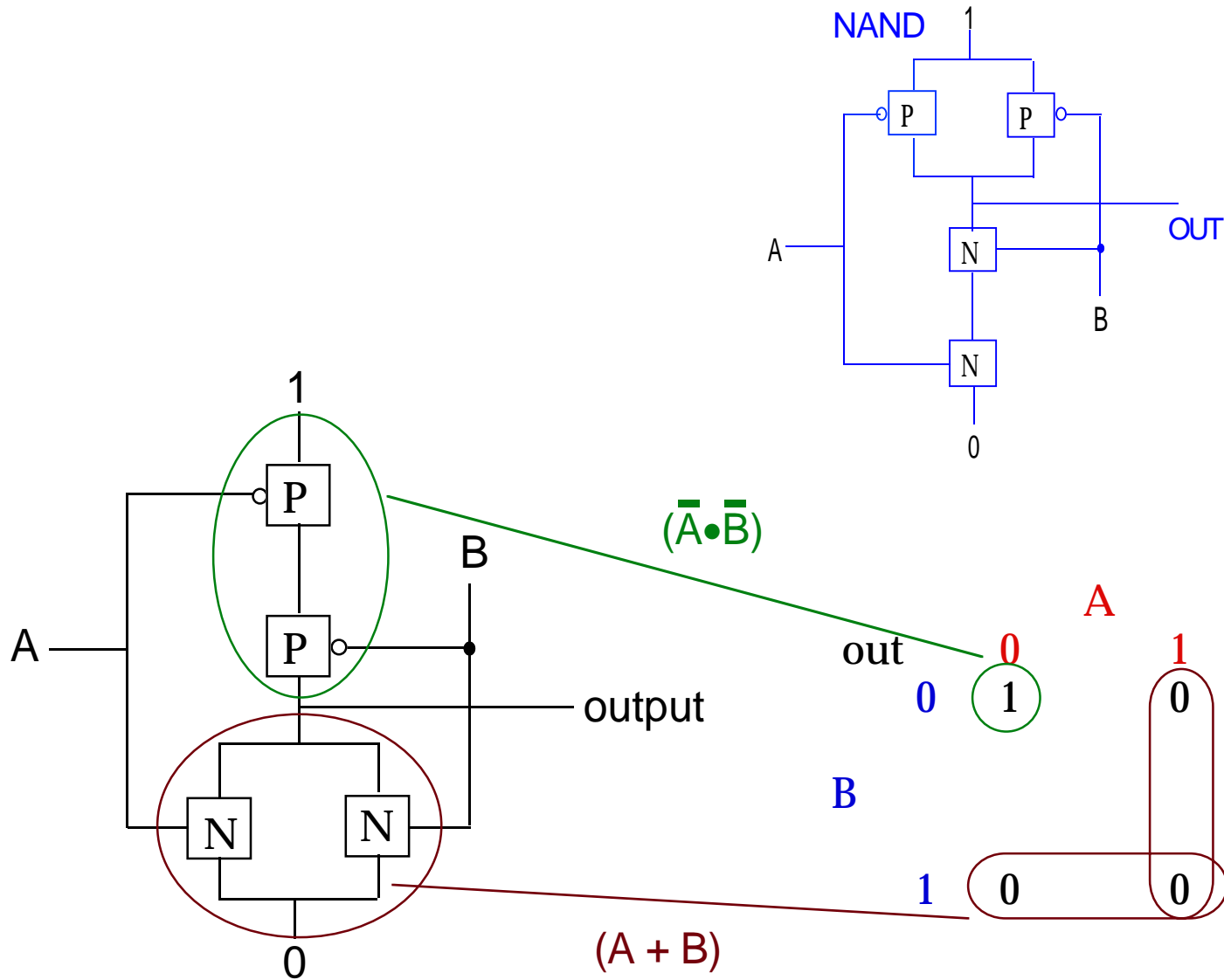
	U		U
1	D	1	D
	Z		Z
U		U	
1	D	Z	D
	Z		0

B-INPUT

1



2-INPUT CMOS NOR GATE

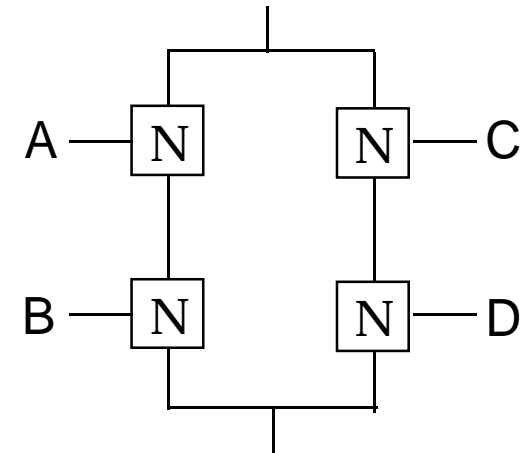
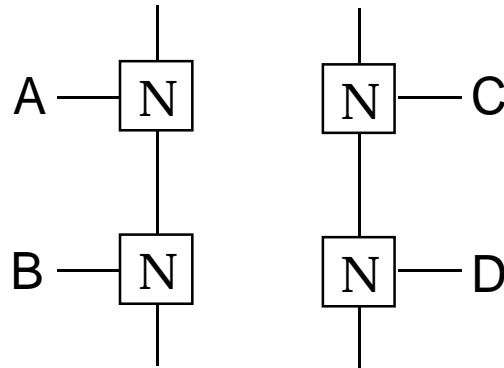


COMPOUND GATES

$$F = \overline{((A \bullet B) + (C \bullet D))}$$

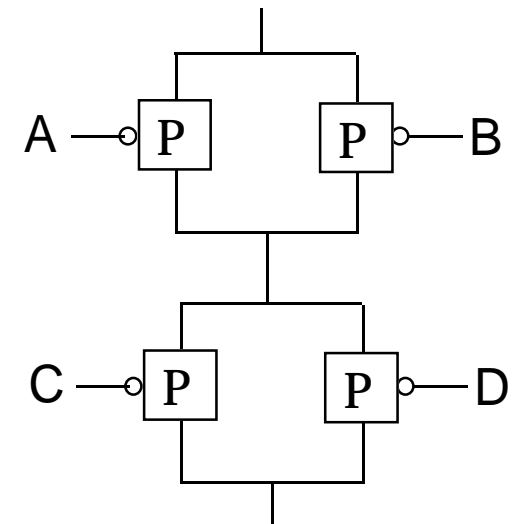
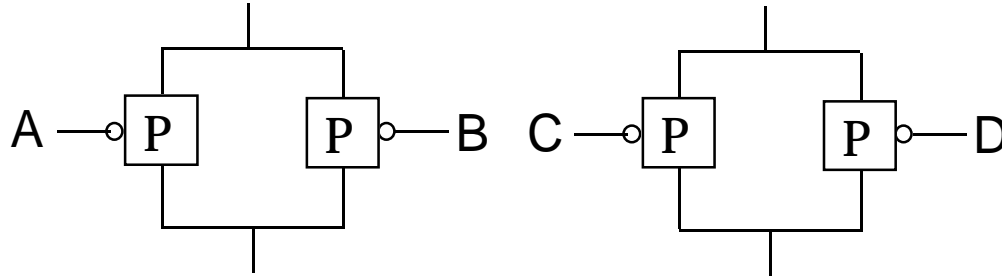
N - Half

$$F = ((A \bullet B) + (C \bullet D))$$

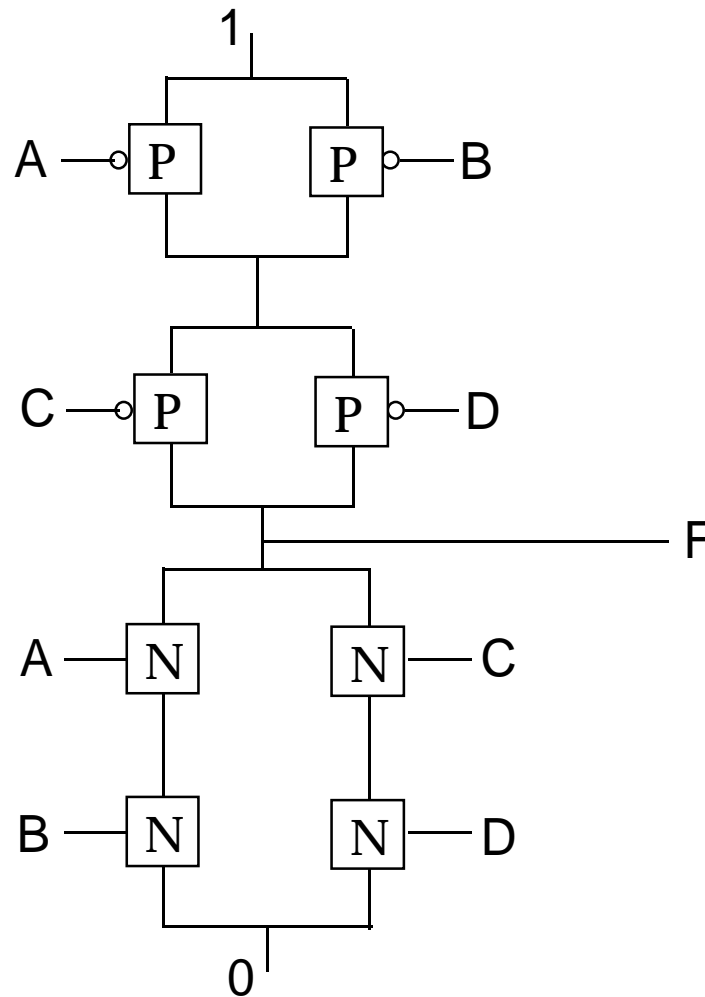


P - Half

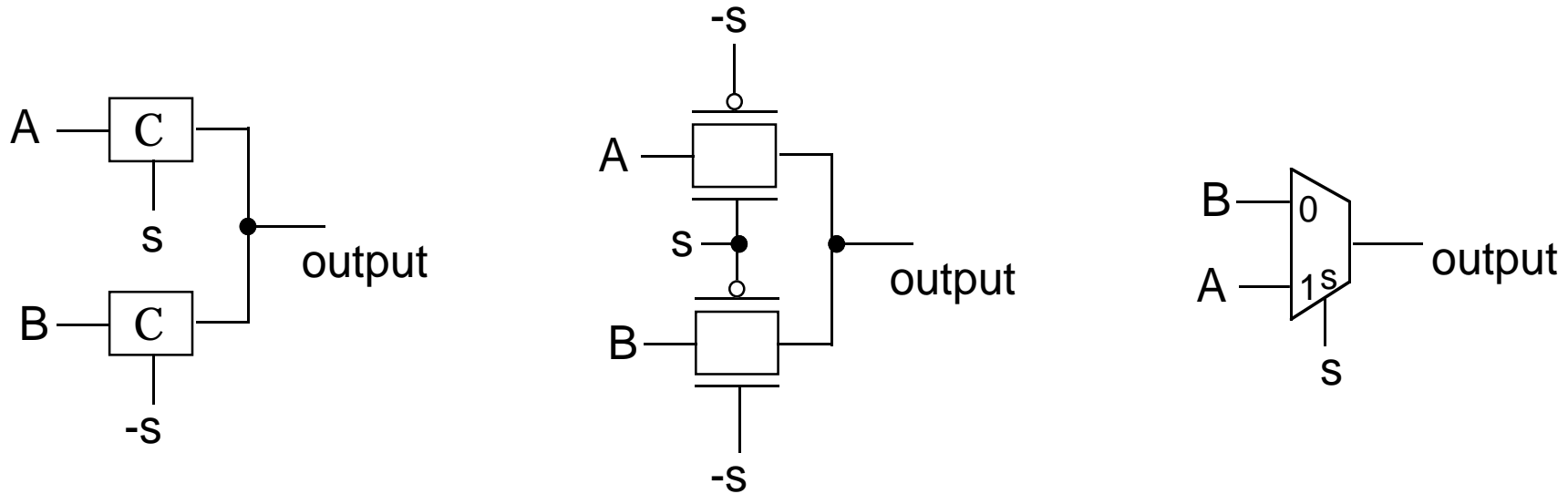
$$F = ((\bar{A} + \bar{B}) \bullet (\bar{C} + \bar{D}))$$



$$F = \overline{((A \cdot B) + (C \cdot D))}$$



2-INPUT MULTIPLEXER



A	B	s	-s	output
x	0	0	1	0 (B)
x	1	0	1	1 (B)
0	x	1	0	0 (A)
1	x	1	0	1 (A)

$$\text{output} = A.s + B.\bar{s}$$

Key components in CMOS memory elements and data manipulation structures.

CIRCUIT AND SYSTEM REPRESENTATIONS

COMPLEX DIGITAL SYSTEM can be SUCCESSIVELY SUB-DIVIDED in a HIERARCHIAL manner.

Highly automated techniques exist for converting HIGH LEVEL DESCRIPTIONS OF SYSTEM BEHAVIOR to a detailed implementation prescription to fabricate a CHIP.

To do this, a set of ABSTRACTIONS have been developed to describe integrated electronic systems.

Designs are represented in THREE distinct DOMAINS:

1. Behavioral: what does the system do?
2. Structural: how are the elements connected together?
3. Physical: how is the structure to be built?

Each DESIGN DOMAIN can be specified at a variety of LEVELS of ABSTRACTION

- Architectural
- Algorithmic
- Module or Functional Block
- Logical
- Switch
- Circuit

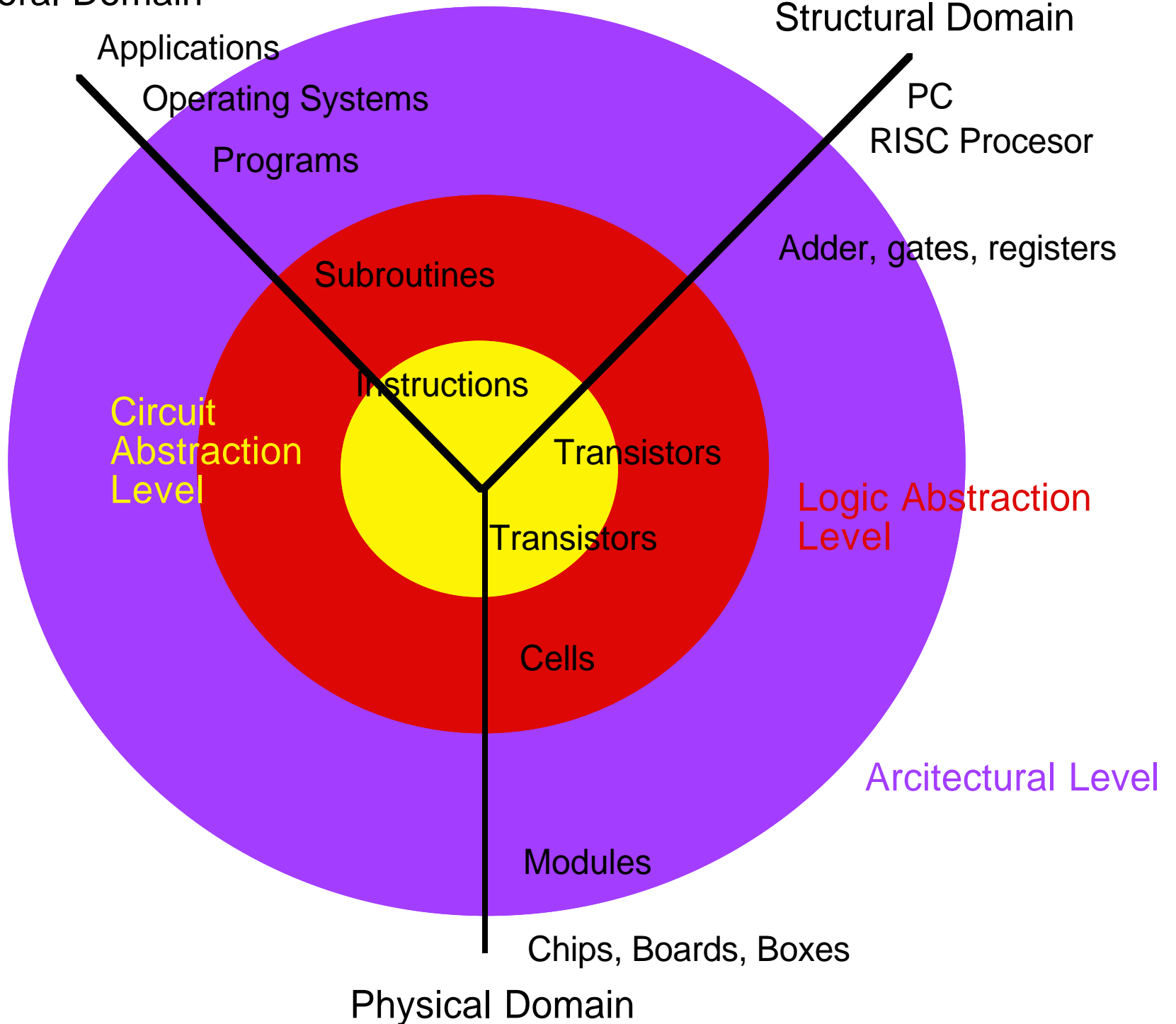
Higher Level



Lower Level

Behavioral Domain

Structural Domain



BEHAVIORAL REPRESENTATION

Behavior may be specified by:

1. Boolean expressions
2. Tables of input/output values
3. Algorithms written in high level computer languages
4. Algorithms written in Hardware Description Languages (HDLs)

e.g. VHDL, Verilog

highest level  lowest level
 Algorithm -> Registers and communications -> -> Boolean expressions

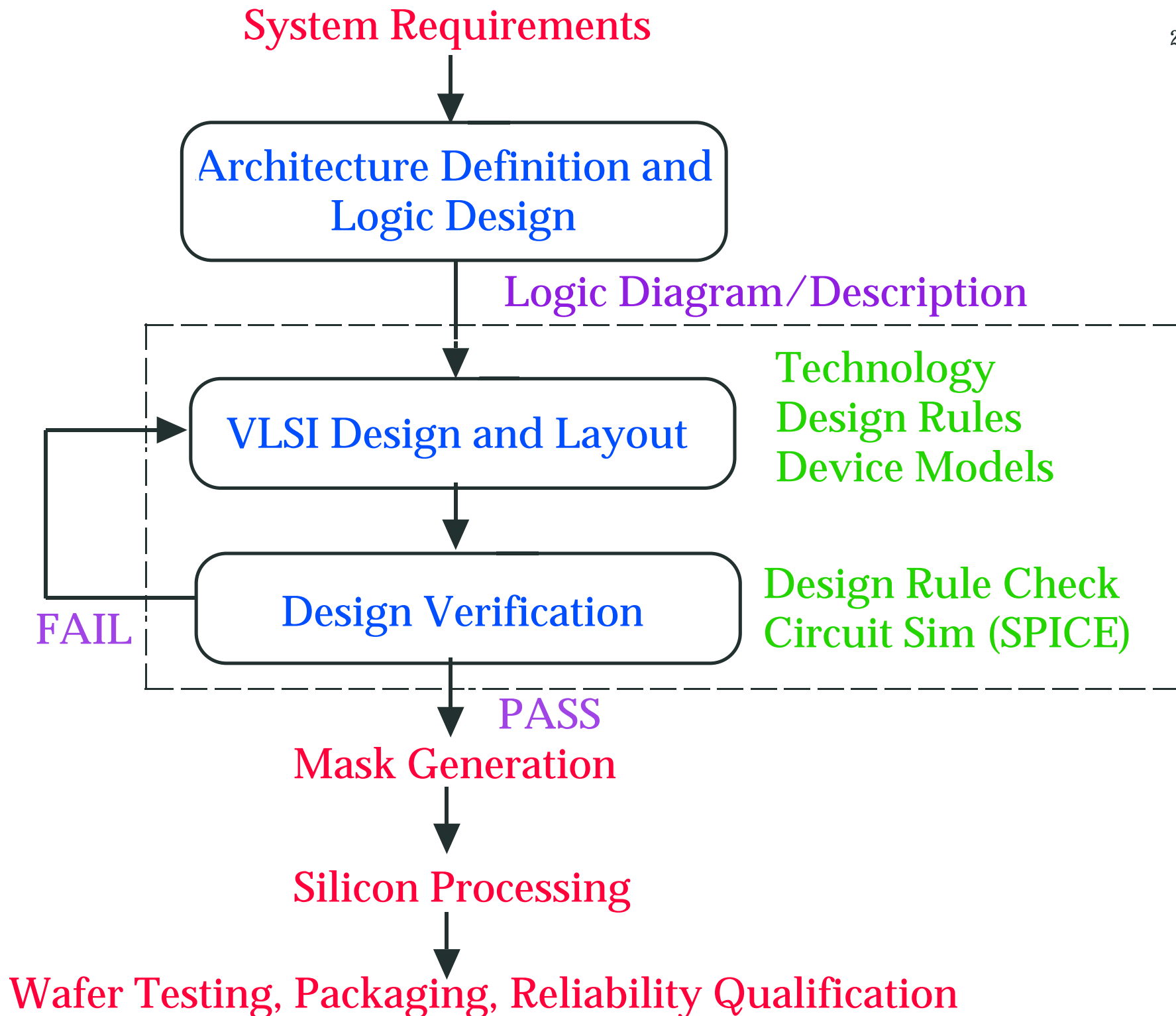
GOAL OF MODERN DESIGN SYSTEMS:

Convert spec at HIGHEST LEVEL possible into a system design in MINIMUM TIME and with MAXIMUM LIKLIHOOD that the design will PERFORM AS DESIRED.

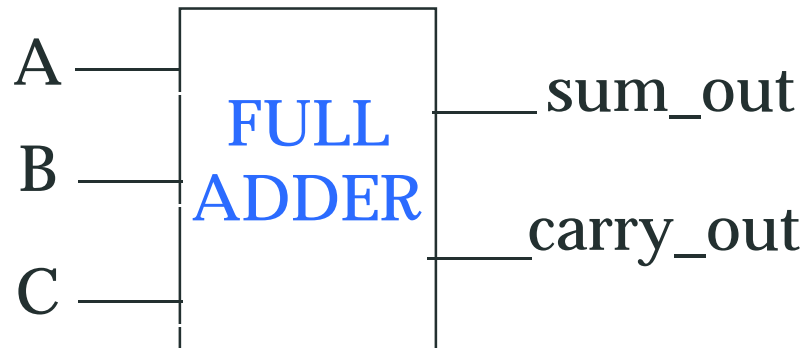
Example 1-1: pp 10

Design a one-bit binary adder circuit using 1 μm n-well CMOS technology. The specifications are:

1. Propagation Delay Times of SUM & CARRY_OUT signals: **< 1.2 ns**
2. Transition Delay Times of SUM & CARRY_OUT signals: **< 1.2 ns**
3. Circuit Die Area: **< 1500 μm^2**
4. Dynamic Power Dissipation (@ $V_{\text{DD}} = 5 \text{ V}$ and $f_{\text{max}} = 20 \text{ MHz}$): **< 1 mW**



START: Boolean description of binary adder circuit:



A	B	C	sum_out	carry_out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

DEFINE:

Input Variables:

addends: A, B

carry-in: C

Output Variables:

sum_out, carry_out

BOOLEAN FUNCTION:

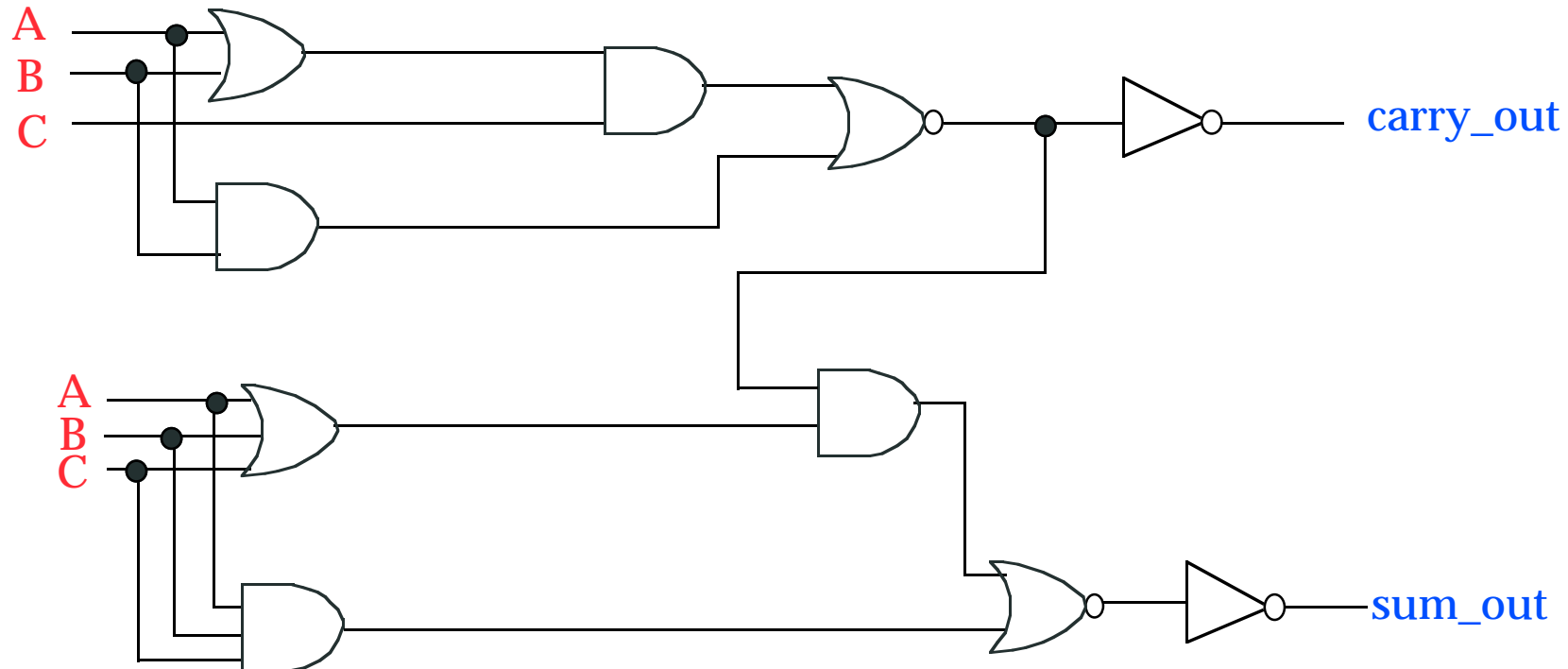
$$\text{sum_out} = A \oplus B \oplus C = ABC + \overline{A}\overline{B}C + \overline{A}B\overline{C} + A\overline{B}\overline{C}$$

$$\text{carry_out} = AB + AC + BC$$

BOOLEAN FUNCTION:

$$\text{SUM_OUT} = A \oplus B \oplus C = ABC + \overline{A}\overline{B}C + \overline{A}B\overline{C} + A\overline{B}\overline{C}$$

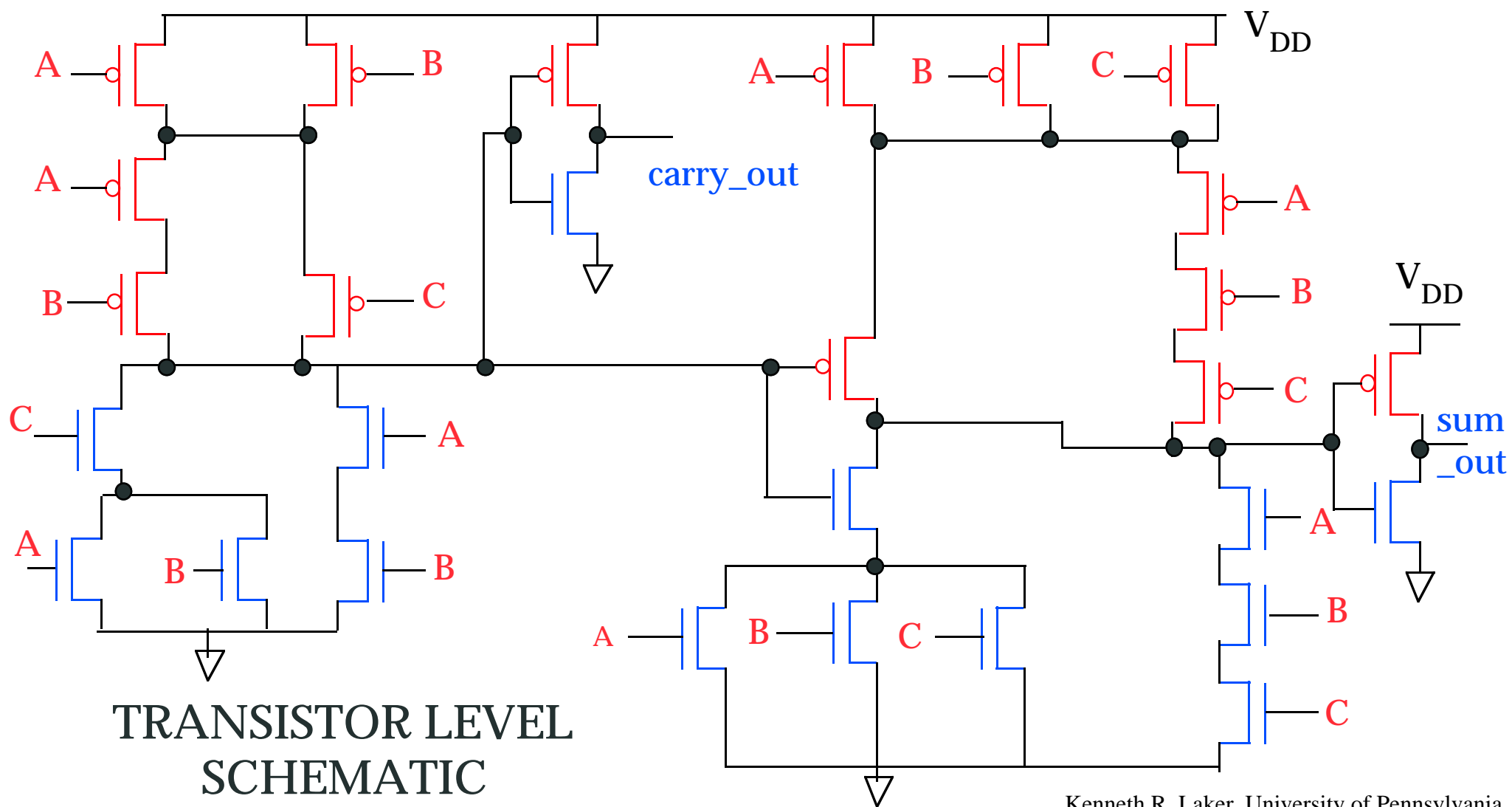
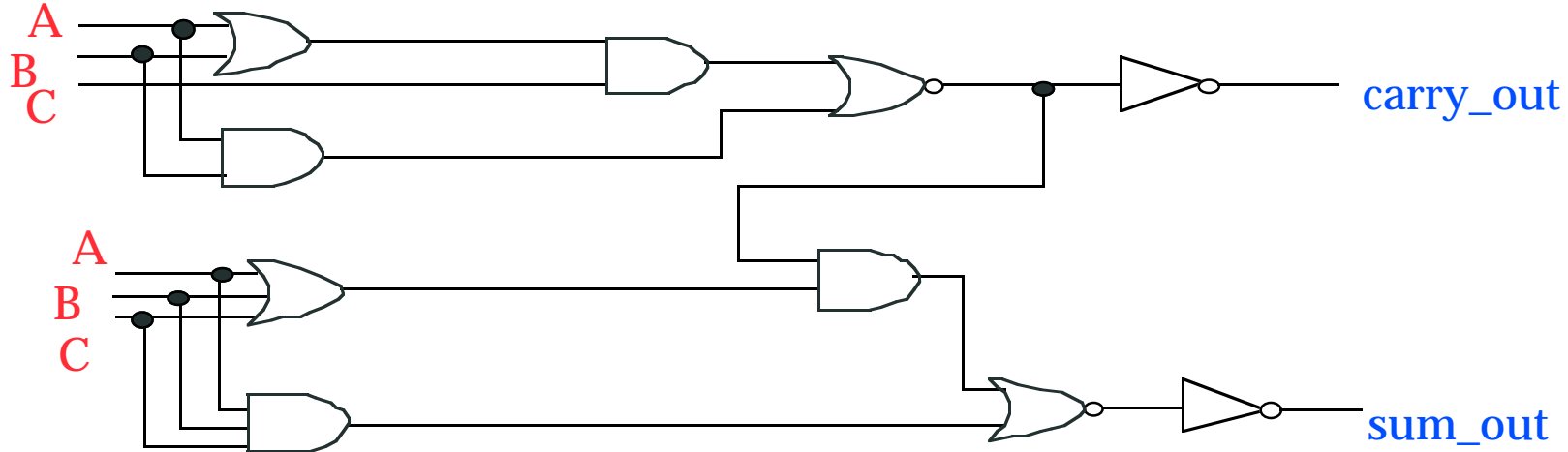
$$\text{CARRY_OUT} = AB + AC + BC$$

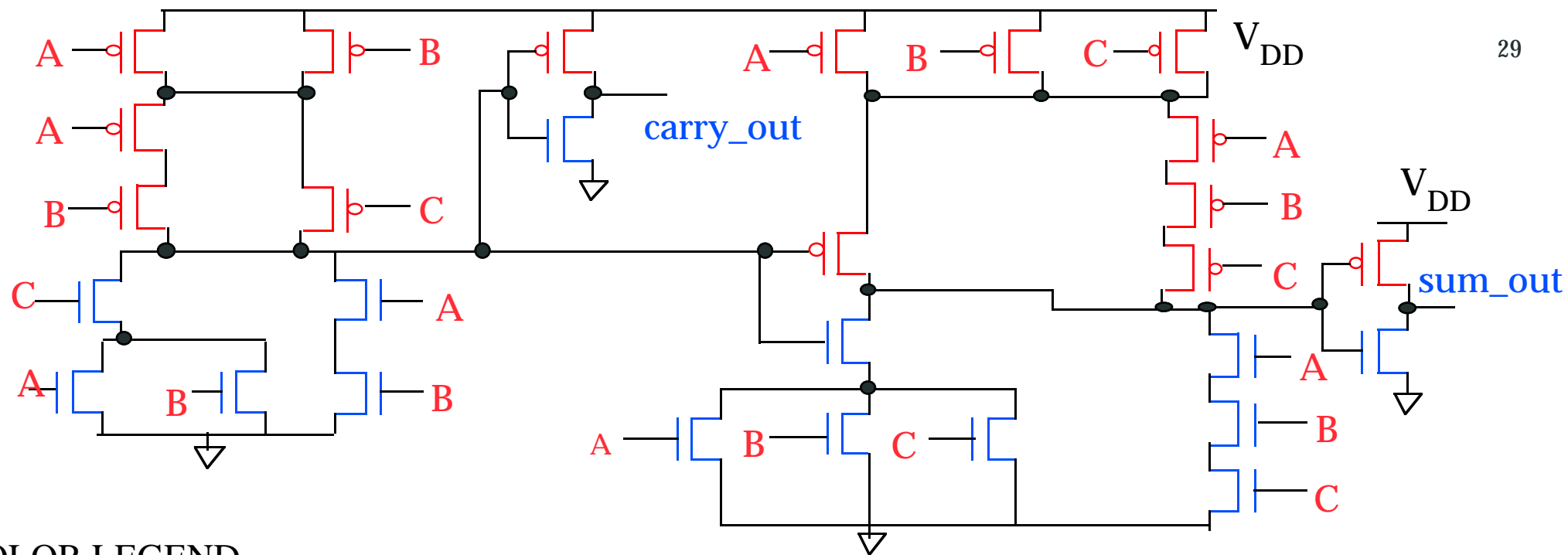


$$\text{SUM_OUT} = ABC + (A + B + C) \overline{\text{CARRY_OUT}}$$

(use of carry_out to realize sum_out reduces circuit complexity and chip area)

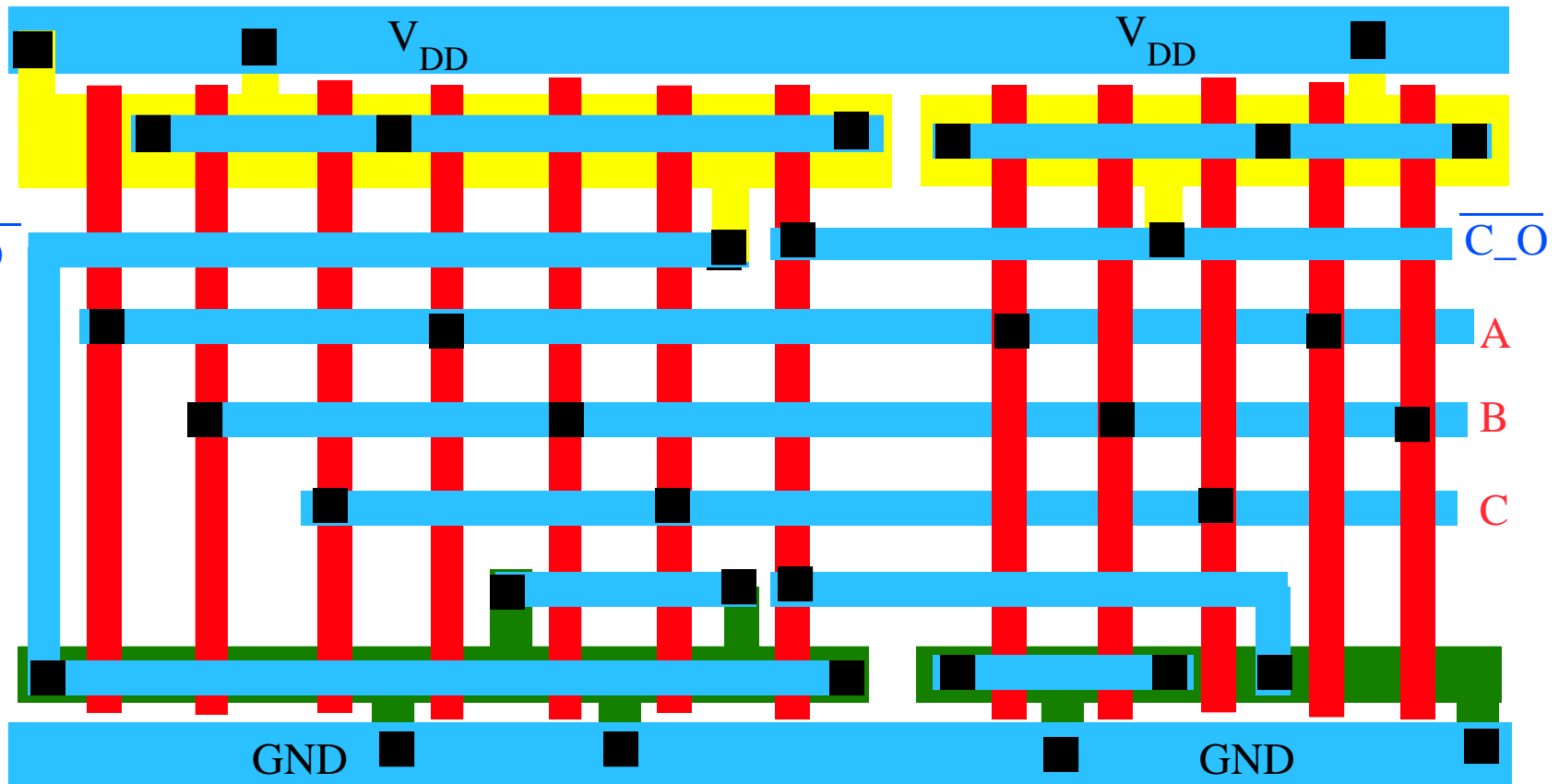
GATE LEVEL SCHEMATIC OF ONE-BIT FULL ADDER CIRCUIT

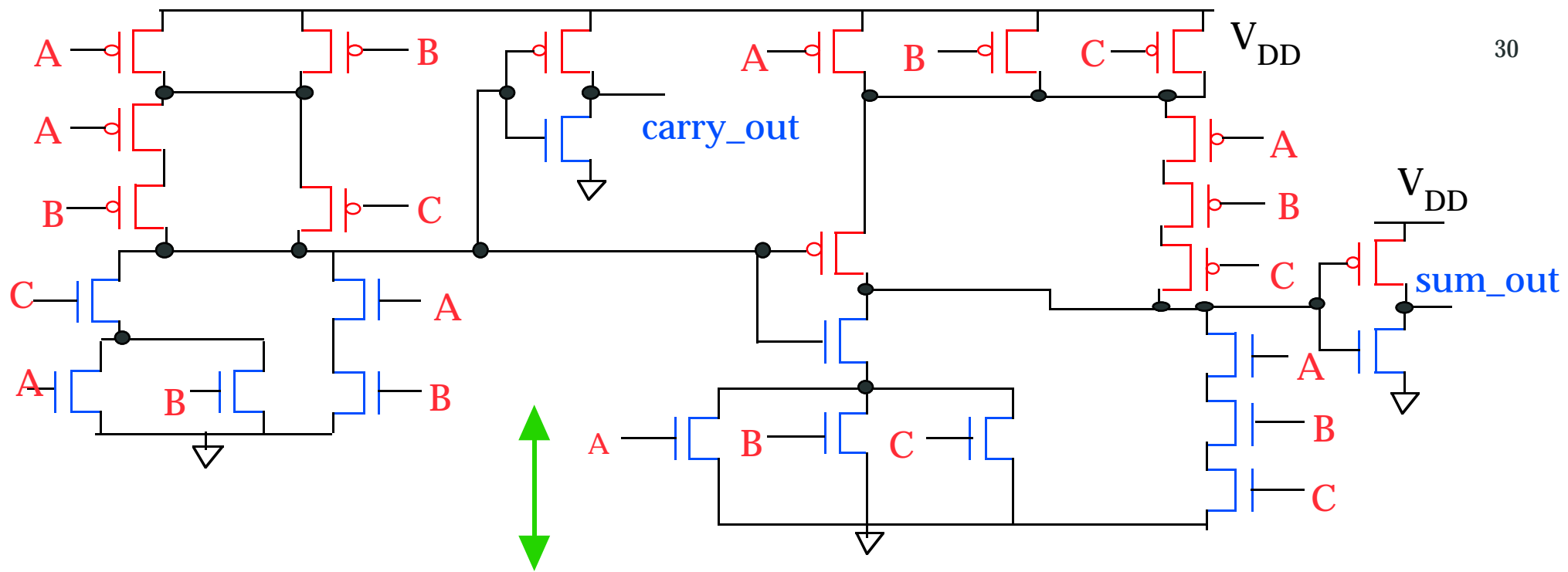




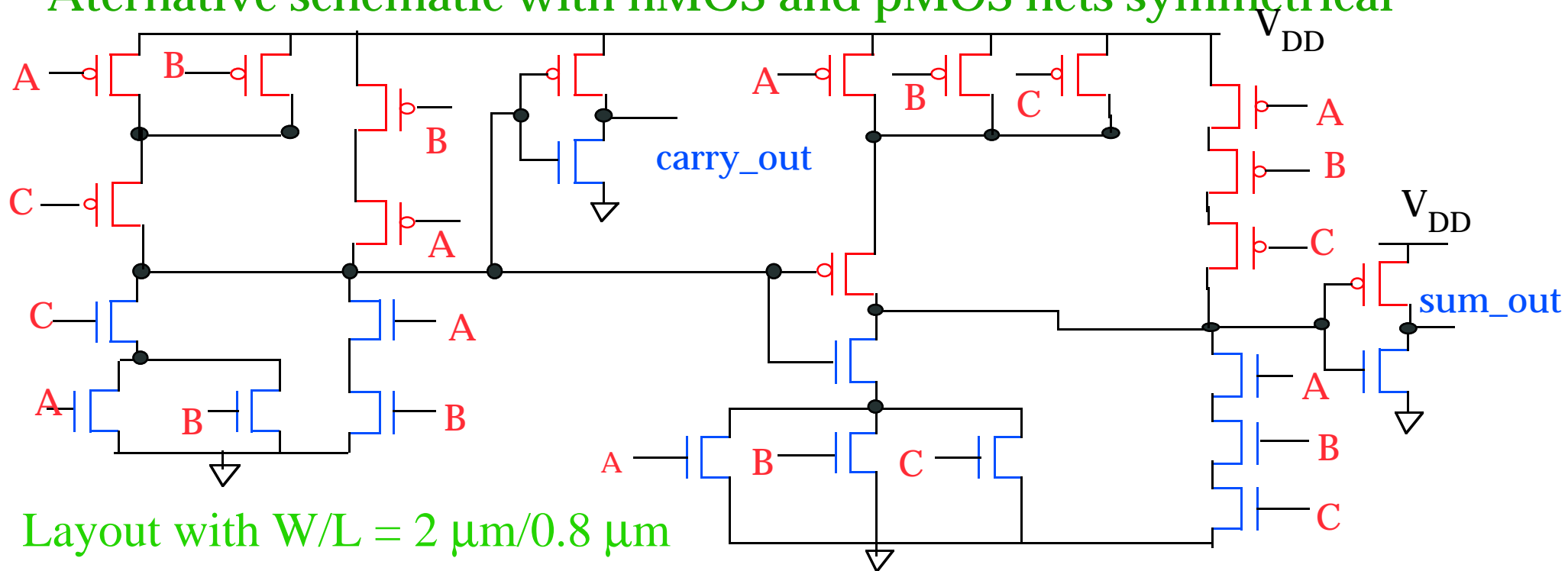
COLOR LEGEND

- n-Well
- p-Well
- n⁺
- Poly
- p⁺
- Gate Oxide
- Field Oxide
- Metal 1
- Metal 2
- Metal 3
- Contact/via





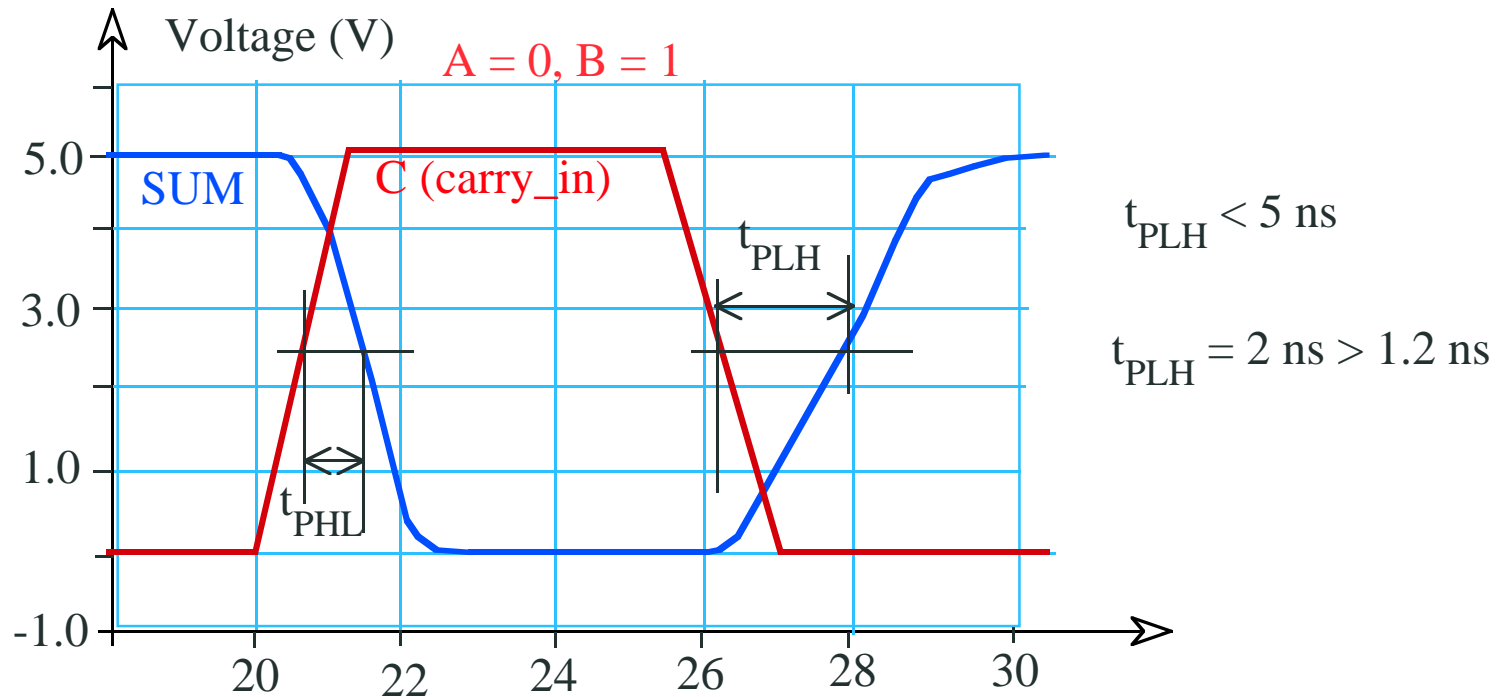
Alternative schematic with nMOS and pMOS nets symmetrical



Layout with $W/L = 2 \mu\text{m}/0.8 \mu\text{m}$

Area $21 \mu\text{m} \times 54 \mu\text{m} = 1134 \mu\text{m}^2$

Layout with $W/L = 2 \mu\text{m}/0.8 \mu\text{m}$



Modified Layout Required

1. Increase W/L 's of transistors
2. Consider more compact placement of transistors and reduce interconnect in critical paths

