Small-Signal Analysis of CMOS Two-Stage Op Amp

- Cascade two-port models of differential amplifier with current-mirror supply (input stage) and common-source amplifier with current supply (second gain stage)

First stage:

- Polarity of $G_{m1}$ is inverted to reflect reversal of input terminals ... which is done to make the overall gain positive for $v_d > 0$

\[
G_{m1} = g_{m1} \\
R_{out1} = r_2 \parallel r_4
\]

Second stage:

\[
G_{m2} = g_{m5} \\
R_{out} = r_5 \parallel r_6
\]

\[
a_{vdo} = (-G_{m1}R_{out1})(-G_{m2}R_{out})
\]

\[
a_{vdo} = g_{m1}(r_2 \parallel r_4)g_{m5}(r_5 \parallel r_6)
\]
Two-Stage CMOS Design Example

- Design constraints

  Typical situation for an internal op amp: area and power are both limited.
  
  Simplified area constraint -- set $W_{\text{max}} = 150 \, \mu\text{m}$
  
  (for minimize channel-length modulation, set $L_{\text{min}} = 3 \, \mu\text{m}$)
  
  Set DC power budget at 1.25 mW (including reference current) for case where we have symmetrical supplies: $V^+ = 2.5 \, \text{V}$ and $V^- = -2.5 \, \text{V}$.

- Initial Transistor Sizing:

  Make $(W/L)_1 = (150 \, \mu\text{m} / 3 \, \mu\text{m})$ in order to maximize $G_{m1}$ and maximize common-mode input voltage range
  
  DC currents: assume $I_{\text{REF}} = 50 \, \mu\text{A}$
  
  Set DC bias current of differential amplifier = DC bias of common-source stage = 100 $\mu$A each as a first-cut --> total current drawn is 250 $\mu$A --> power spec. is just met
  
  Transistor dimensions: $(W/L)_5 = (150 \, \mu\text{m} / 3 \, \mu\text{m})$ to maximize $g_{m5}$
  
  \[
  \frac{(W/L)_5}{2(W/L)_{3,4}} = \frac{-I_{D6}}{I_{D7}} = \frac{100 \, \mu\text{A}}{100 \, \mu\text{A}} = 1
  \]
  
  Therefore $(W/L)_{3,4} = (W/L)_5 / 2 = 25$ --> $W_{3,4} = 75 \, \mu\text{m}$ since we use $L_{\text{min}}$ to save area.
  
  For symmetrical output swing, we set $(W/L)_6 = (W/L)_5 = (150 \, \mu\text{m} / 3 \, \mu\text{m})$
  
  To maximize common-mode input range, we also set $(W/L)_7 = (150 \, \mu\text{m} / 3 \, \mu\text{m})$
First-Cut CMOS Two-Stage Op Amp

\[ \begin{align*}
M_8 \quad & (75/3) \\
M_7 \quad & (150/3) \\
\rightarrow M_1 \quad & (150/3) \\
\rightarrow M_2 \quad & (150/3) \\
\rightarrow M_3 \quad & (75/3) \\
\rightarrow M_4 \quad & (75/3) \\
\rightarrow M_5 \quad & (150/3) \\
M_6 \quad & (150/3) \\
\rightarrow +2.5 \ V \\
\rightarrow -2.5 \ V \\
\end{align*} \]

\[ \begin{align*}
50 \ \mu A \\
\gamma_n = 0.6 \ \text{V}^{1/2} \\
\gamma_p = 0.6 \ \text{V}^{1/2} \\
\end{align*} \]

n-channel MOSFET

\[ \begin{align*}
\mu_n C_{ox} &= 50 \ \frac{\mu A}{V^2} \\
t_{ox} &= 15 \ \text{nm} \\
V_{TOn} &= 1.0 \ \text{V} \\
\lambda_n &= \frac{0.1(\mu m/V)}{L} \\
&= \frac{0.1(\mu m/V)}{L} \\
\gamma_n &= 0.6 \ \text{V}^{1/2} \\
2\phi_p &= -0.8 \ \text{V} \\
C_{ov} &= 0.5 \ \text{fF}/\mu m \\
\phi_{Bn} &= 0.95 \ \text{V} \\
m_jn &= 0.5 \\
C_{jwno} &= 0.5 \ \text{fF}/\mu m \\
m_{jw} &= 0.33
\end{align*} \]

p-channel MOSFET

\[ \begin{align*}
\mu_p C_{ox} &= 25 \ \frac{\mu A}{V^2} \\
t_{ox} &= 15 \ \text{nm} \\
V_{TOP} &= -1.0 \ \text{V} \\
\lambda_p &= \frac{0.1(\mu m/V)}{L} \\
&= \frac{0.1(\mu m/V)}{L} \\
\gamma_p &= 0.6 \ \text{V}^{1/2} \\
2\phi_n &= 0.8 \ \text{V} \\
C_{ov} &= 0.5 \ \text{fF}/\mu m \\
\phi_{Bp} &= 0.95 \ \text{V} \\
m_jp &= 0.5 \\
C_{jwpo} &= 0.35 \ \text{fF}/\mu m \\
m_{jwp} &= 0.33
\end{align*} \]
DC Bias Solution

- Assume that the DC input voltages are $V_{I+} = V_{I-} = 0$ V and $V_O = 0$ V

- Input common-mode voltage range

$$V_{IC,max} = 2.5 \text{ V} - (-1 \text{ V}) - 1.28 \text{ V} - 1.4 \text{ V} = 0.82 \text{ V}$$

$$V_{IC,min} = -2.5 \text{ V} + 1.28 \text{ V} + (-1 \text{ V}) = -2.22 \text{ V}$$

room for improvement in the upper limit -- possible at the expense of increased area ($W/L$) ratios must be increased.

- Output voltage swing

$$V_{O,max} = 2.5 \text{ V} - 0.4 \text{ V} = 2.1 \text{ V}$$

$$V_{O,min} = -2.5 \text{ V} + 0.28 \text{ V} = -2.22 \text{ V}$$

output range in nearly symmetrical and adequate
Small-Signal Performance

- Small-signal parameters:
  
  \[ g_{m1} = g_{m2} = 357 \, \mu\text{S} \]
  
  \[ g_{m5} = 2 \, g_{m1} = 714 \, \mu\text{S} \]
  
  \[ r_{o2} = r_{o4} = 600 \, \text{k}\Omega \]
  
  \[ r_{o5} = r_{o6} = 300 \, \text{k}\Omega \]

- Differential voltage gain:

  \[ a_{vdo} = (0.357)(600\parallel600)(714\parallel300) = 1.15\times10^4 \]

  in decibels, \( |a_{vdo}|_{\text{dB}} = 81 \, \text{dB} \).
Stability -- A Brief Introduction

- Non-inverting, unity gain configuration

\[ v_s(t) = v_s \sin(\omega_s t) \]

Feedback is to negative terminal of op amp, which tends to stabilize the output voltage \( v_o(t) \) to be nearly equal to \( v_s(t) \)

- What happens when the phase of \( a_{vd}(j\omega_s) = 180^\circ \)?
  
  ... the sign of \( a_{vd} \) is flipped! Consider + and - terminals to be reversed!
  
  ... if \(|a_{vd}(j\omega_s)| > 1\), then the output is *destabilized* if the input is perturbed.
Ensuring Stability

- If the gain of the op amp is less than 1 (in magnitude) when the phase is $180^\circ$, then the unity-gain non-inverting configuration (worst-case) will be stable.

- One solution: locate the second pole of the op amp $\omega_2$ at approximately the unity gain frequency

  $$\omega_2 \approx a_{vdo} \omega_1$$

- The second gain stage is responsible for both poles

  ![Diagram](image)

Device capacitances are lumped together in the circuit:

\[
C_1 = C_{gs5} + C_{gd4} + C_{db4} + C_{gd2} + C_{db2} \\
C_L' = C_L + C_{db5} + C_{db6} + C_{gd6} \\
C_c' = C_c + C_{gd5}
\]

The compensation capacitor $C_c$ sets the dominant pole $\omega_1$ by the Miller effect:

$$\omega_1^{-1} \approx R_1 C_1 + R_1 (1 + G_{m2} R_{out}) C_c'$$

where $R_1 = R_{out1}$
Second Pole Location

- Direct factoring of transfer function --> “exact” expression for $\omega_2$

For the case when $C_1 \ll C'_c, C'_L$

$$\omega_2 \approx \frac{G_{m2}}{C'_L} = \frac{1}{(1/G_{m2})C'_L}$$

- Interpretation:

At frequencies around $\omega_2 (\gg \omega_1)$, the impedance $Z_c = (1 / j\omega_2 C_c)$ is small enough that $M_5$ can be considered diode-connected.

Load capacitance sees a Thévenin resistance of $1 / g_{m5}$ --> $\omega_2$ is set by the load capacitance in parallel with $1 / g_{m5}$

- Adjusting compensation and load capacitors to satisfy $\omega_2 \approx a_{vdo} \omega_1$

$$\omega_2 \approx \frac{G_{m2}}{C'_L} \approx \frac{(G_{m1}R_{out1})(G_{m2}R_{out})}{R_1 C_1 + R_1 (1 + G_{m2}R_{out})C_c} \approx \frac{(G_{m1}R_{out1})(G_{m2}R_{out})}{G_{m2}R_1 R_{out} C'_c}$$

since $G_{m2}R_{out} \gg 1$

$$C'_c \approx C'_L \left(\frac{G_{m1}}{G_{m2}}\right)$$
Capacitor Sizing

- The load capacitor is set by system specifications: $C_L = 7.5$ pF
  with parasitic capacitances --> $C_L' = C_L + 350$ fF $= 7.85$ pF

- The compensation capacitor is approximately

$$
C_c' \approx \left( \frac{357 \ \mu S}{714 \ \mu S} \right) C_L' = 3.9 \text{ pF}
$$

the “exact” result is significantly higher ... $C_c' = 5.3$ pF

- Area requirement with a 500 Å thick oxide is less than 100 x 100 μm² -->
  not a significant addition to the op amp area

- Pole locations:

$$
\omega_1 = 5.8 \text{ krad/s} \quad \omega_2 = 67.2 \text{ Mrad/s}
$$

- SPICE: must increase $C_c$ to 20 pF in order to have $\omega_2 \approx a_{vdo} \omega_1$

$$
\omega_1 = 1.3 \text{ krad/s} \quad \omega_2 = 10.4 \text{ Mrad/s}
$$