**BiCMOS Two-Stage Operational Amplifier**

- Increased second-stage transconductance --> boost second pole location

First cut: replace $M_3, M_4, M_5$ by $Q_3, Q_4, Q_5$

(note that npn bipolar current mirror is necessary to avoid a systematic input offset voltage)
First-Cut BiCMOS Two-Stage Op Amp (Cont.)

- Drawback to first-cut design

\[ a_{vdo} = g_{m1}(r_o^2) \left| r_o^4 \right| r_{\pi5} g_{m5}(r_o^5) \left| r_o^6 \right| \]

since the input resistance of the common-emitter is much smaller than the output resistance of the input stage

\[ a_{vdo} \approx g_{m1} r_{\pi5} g_{m5}(r_o^5) \left| r_o^6 \right| \]

- Reduced low-frequency gain is unacceptable
Improved BiCMOS Two-Stage Op Amp

- Increase input resistance of the second stage: insert a common-collector device $Q_{11}$ and associated biasing transistors $M_{12}, M_{13},$ and $M_{14}$.

- DC level of $M_2$’s drain is increased by $V_{BE11}$ --> must add $Q_9$ and $Q_{10}$ to avoid a systematic input offset.
Small-Signal Performance

- Low-frequency gain is increased:

\[ a_{vdo} = A_{dm1}A_{v, cc}A_{v, ce} = (-g_m r_o2 | \beta_o r_o10) A_{v, cc} (g_m5 r_o5 | r_o6) \]

- The common-collector gain is \( A_{v, cc} = v_o/v_{b5} \) and is about 1

\[ a_{vdo} \approx g_m1 r_o2 g_m5 (r_o5 | r_o6) \]

low-frequency gain is much higher than first-cut BiCMOS design
Improved BiCMOS Two-Stage Design

- Minimize power --> set $I_{C11} = 25 \mu A$

![Diagram of a BiCMOS two-stage design]

**Vertical npn bipolar transistor**

- $\beta_F = \beta_o = 100$
- $r_b = 250 \Omega$
- $C_{je0} = 8 \text{ fF}$
- $m_{je} = 0.5$
- $\phi_{Be} = 0.95 \text{ V}$
- $I_S = 10^{-17} \text{ A}$
- $r_c = 200 \Omega$
- $C_{j\mu o} = 22 \text{ fF}$
- $m_{jc} = 0.5$
- $\phi_{Bc} = 0.79 \text{ V}$
- $V_{An} = 25 \text{ V}$
- $r_{ex} = 5 \Omega$
- $C_{cso} = 41 \text{ fF}$
- $m_{js} = 0.5$
- $\phi_{Bs} = 0.71 \text{ V}$
- $\tau_F = 50 \text{ ps}$
Small-Signal Performance and Frequency Response

- Low-frequency differential gain

\[ a_{vdo} = A_{d1} A_{v,cc} A_{v,ce} = (-212)(0.78)(-525) = 86,800 \]

in decibels \( |a_{vdo}|_{dB} = 99 \) dB

- Second stage transconductance (composite CC/CE amplifier)

\[ G_{m2} \approx g_m = \frac{I_{C5}}{V_{th}} = 3.85 \text{ mS} \]

which is a factor of 10 higher than for the CMOS two-stage amplifier

As a result, the compensation capacitor is reduced to

\[ C_c = \left( \frac{G_{m1}}{G_{m2}} \right) C_L' = \left( \frac{0.357 \text{ mS}}{3.85 \text{ mS}} \right)(7.77 \text{ pF}) = 720 \text{ fF} \]

The “exact” result is \( C_c = 980 \text{ fF} \)

- Dominant pole

\[ \omega_1 = \frac{1}{(R_{out1} || R_{out2}) G_{m2} R_{out} C_c} = 3.3 \text{ krad/s} \]

\[ \omega_2 \approx a_{vdo} \omega_1 \approx 300 \text{ Mrad/s} \ldots \text{which is much higher than for the CMOS op amp} \]
Simulation of Frequency Response

- SPICE indicates that higher frequency poles reduce the unity-gain frequency
  Increasing the compensation capacitor to $C_c = 1.3 \text{ pF}$ results in $\omega_2 = a_{vdo} \omega_1$
  $\omega_1 = 2.6 \text{ krad/s}$ and
  $\omega_2 \approx 240 \text{ Mrad/s}$

- BiCMOS op amp has a unity-gain bandwidth that is over 10 times greater than the CMOS op amp, at the cost of
  1. use of a more complex (and expensive) BiCMOS technology
  2. greater area
  3. slightly higher DC power
Op Amp Bode Plots

![Bode plot diagram showing improved BiCMOS and two-stage CMOS op amps]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>CMOS</th>
<th>Improved BiCMOS</th>
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<tbody>
<tr>
<td>Transistor Count*</td>
<td>8</td>
<td>14</td>
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<tr>
<td>Static Power</td>
<td>1.25 mW</td>
<td>1.5 mW</td>
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<tr>
<td>Gain $a_{\text{vlo}}$</td>
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<td>99.9 dB</td>
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<tr>
<td>$V_{I_C,\text{max}}$</td>
<td>0.82 V</td>
<td>0.82 V</td>
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<tr>
<td>$V_{I_C,\text{min}}$</td>
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<td>$-2.1$ V</td>
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<tr>
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<td>2.1 V</td>
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<tr>
<td>$V_{O,\text{min}}$</td>
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<td>$-2.4$ V</td>
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<tr>
<td>$C_c$</td>
<td>20 pF</td>
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<td>$f_1$</td>
<td>202 Hz</td>
<td>410 Hz</td>
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<tr>
<td>$f_2$</td>
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<td>38.3 MHz</td>
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</tbody>
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*not counting the reference current source.